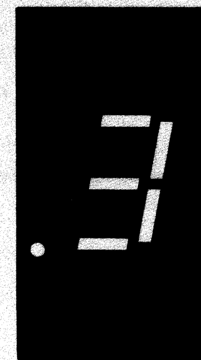
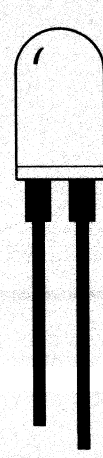
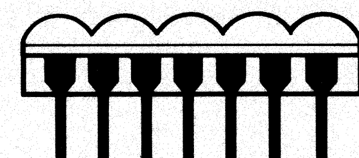
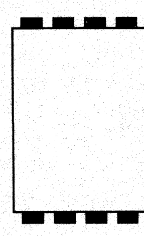
Hewlett
Packard
Components

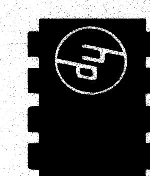




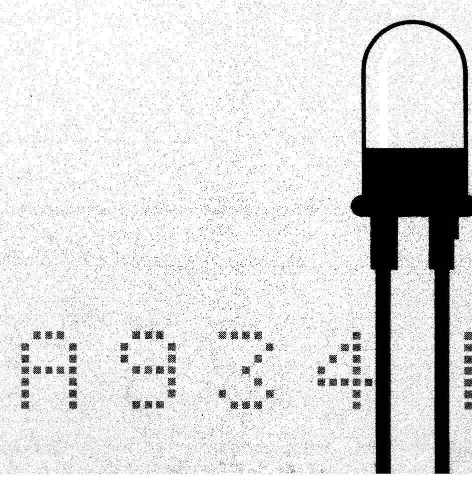




Solid State Display and Optoelectronics Designer's Catalog



July 1973



Hewlett-Packard -- A Brief Sketch

Hewlett-Packard is one of the world's leading designers and manufacturers of electronic, medical, analytical, and computing instruments and systems, diodes, transistors, and optoelectronic products. From its founding in 1939, the company has conscientiously followed its basic philosophy of offering only products representing significant technological advancements.

To maintain its leadership in instrument and component technology, Hewlett-Packard invests heavily in new product development. Research and development expenditures traditionally average about 10 percent of sales revenue, and 1,500 engineers and scientists are assigned the responsibilities of carrying out the company's various R and D projects. As a result of this effort, about half of the company's current business is represented by products that were not in existence six years ago.

Hewlett-Packard is a well-established, multinational company that has controlled its growth so that expansion is financed generally from income on a pay-as-you-go basis. From its modest beginnings in Palo Alto, California, the company now has ten manufacturing plants in California, two in Colorado, and one each in Massachusetts, New Jersey, and Pennsylvania. Hewlett-Packard overseas manufacturing facilities are located in Scotland, German Federal Republic, France, Japan, Singapore, and Malaysia.

However, for the customer, Hewlett-Packard is no farther away than the nearest telephone. There are 172 HP sales and service offices located in 65 countries around the world.

These field offices are staffed by trained engineers, each of whom has the primary responsibility of providing technical assistance and data to customers. A vast communications network has been established to link each field office with the factories and with corporate offices. No matter what the product or the request, a customer can be accommodated by a single contact with the company.

Hewlett-Packard is guided by a set of written objectives. One of these is "to provide products and services of the greatest possible value to our customers". Through application of advanced technology, efficient manufacturing, and imaginative marketing, it is the customer that the more than 24,000 Hewlett-Packard people strive to serve. Every effort is made to anticipate the customer's needs, to provide the customer with products that will enable more efficient operation, to offer the kind of service and reliability that will merit the customer's highest confidence, and to provide all of this at a reasonable price.

To better serve its many customers' broad spectrum of technological needs, Hewlett-Packard publishes several catalogs. Among these are:

- Electronic Instruments and Systems for Measurement/Computation (General Catalog)
- DC Power Supply Catalog
- Medical Instrumentation Catalog
- Analytical Instruments for Chemistry Catalog
- Coax. and W/G Measurement Accessories Catalog
- Diode and Transistor Catalog

All catalogs are available at no charge from your local HP sales office.

Hewlett Packard Optoelectronics

A decade of intensive solid state research, the development of advanced manufacturing techniques and continued expansion has enabled Hewlett-Packard to become a high volume supplier of quality, competitively priced LED displays, LED lamps, isolators, and photodetectors.

In addition to our broad product line, Hewlett-Packard also offers the following services: immediate delivery from any of our authorized stocking distributors, applications support, special and QA testing, and a one year guarantee on all of our optoelectronic products.

This package of products and services has enabled Hewlett-Packard to become a recognized leader in the optoelectronic industry.

Catalog Introduction

The new Solid State Display and Optoelectronics Designer's Catalog contains detailed, up-to-date specifications and applications information* on our complete optoelectronic product line. It is divided into the following major product sections: Photodetectors, Isolators, LED Lamps, and LED Displays.

How To Use This Catalog

For your convenience and easy use of this catalog, we have incorporated three methods for locating components: a Table of Contents that allows you to locate components by their general description, a Numeric Index that lists all components by part number, and a Selection Guide for each product group giving a brief overview of the product line.

How To Order Devices

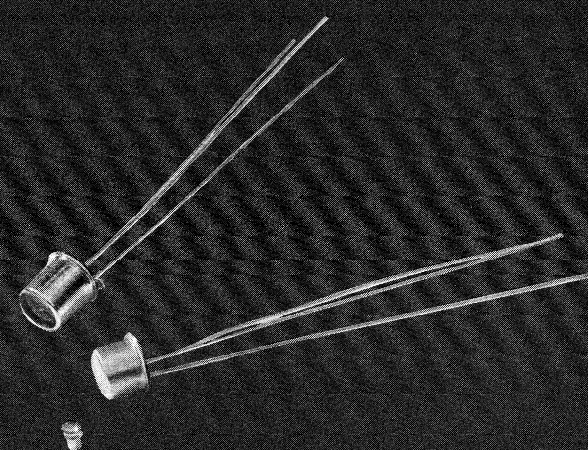
All of our high quality, competitively priced components may be ordered through any of our Sales and Service Offices listed on the back cover of this catalog. In addition, for immediate delivery of Hewlett-Packard optoelectronic components, contact any of the worldwide stocking distributors listed on the inside back cover of this catalog.

*Hewlett-Packard assumes no responsibility for the use of any circuits described herein and makes no representations or warranties, express or implied, that such circuits are free from patent infringement.

Table of Contents

Numeric Index

Photodetectors

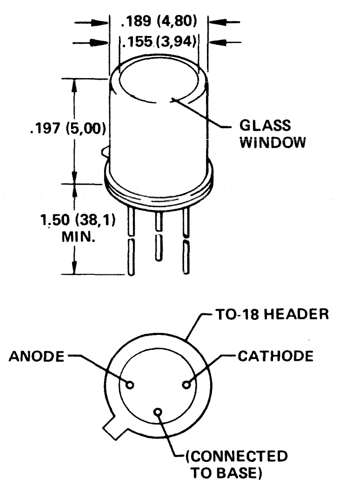


Photodetectors (PIN Photodiode)

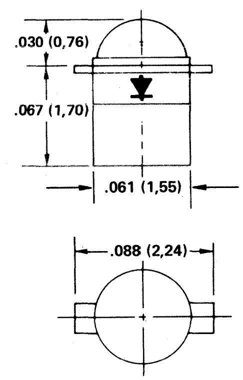
FEATURES	• High Speed — 1 ns Speed of Response • Wide Dynamic Range — dc to 1 GHz
BENEFITS	• Allows Detection of Fast Light Sources, e.g., Lasers • Applicable to Many Different Light Sources
APPLICATIONS	• Detection of IR Radiation • Card Readers • Tape Readers • Isolators (For further information see Application Note 915, page 7)

HEWLETT hp PACKARD
COMPONENTS

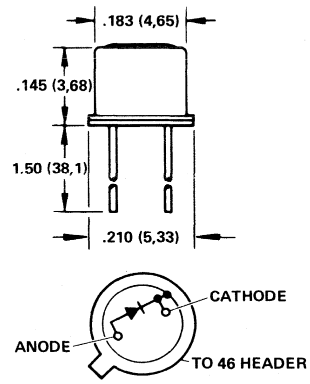
PIN PHOTODIODE HP 5082-4200 series



HP 5082-4203, -4204, -4207



HP 5082-4205



HP 5082-4220

All dimensions in inches and (millimeters)

The HP silicon planar PIN photodiodes are ultrafast light detectors for visible and near infrared radiation. Their response to blue and violet is unusually good for low dark current silicon photodiodes.

The speed of response of these detectors is less than one nanosecond. Laser pulses shorter than 0.1 nanosecond may be observed. The frequency response extends from dc to 1 GHz.

The low dark current of these planar diodes enables detection of very low light levels. The quantum detection efficiency is constant over six decades of light intensity, providing an excellent dynamic range.

The 5082-4203, -4204, and -4207 are packaged on a standard TO-18 header with a plane glass window cap. For versatility of circuit connection, they are electrically insulated from the header. The light sensitive area of the 5082-4203 and -4204 is 0.020 inch (0,508 mm) in diameter and is located 0.075 inch (1,905 mm) behind the window. The light sensitive area of the 5082-4207 is 0.040 inch (1,016 mm) in diameter and is also located 0.075 inch (1,905 mm) behind the window.

The 5082-4205 is in a low capacitance Kovar and ceramic package of very small dimensions, with a hemispherical lens.

The 5082-4220 is packaged on a TO-46 header with the 0.020 inch (0,508 mm) diameter sensitive area located 0.100 inch (2,540 mm) behind a flat glass window.

NOISE FREE PROPERTIES

The noise current of the PIN diodes is negligible. This is a direct result of the exceptionally low leakage current, in accordance with the shot noise formula $I_N = (2qI_R\Delta f)^{1/2}$. Since the leakage current does not exceed 400 picoamps for the 5082-4204 at a reverse bias of 10 volts, shot noise current is less than 1.2×10^{-14} amp $Hz^{-1/2}$ at this voltage.

Excess noise is also very low, appearing only at frequencies below 10 Hz, and varying approximately as 1/f. When the output of the diode is observed in a load, thermal noise of the load resistance (R_L) is $1.28 \times 10^{-10} (R_L)^{-1/2} \times (\Delta f)^{1/2}$ at 25°C, and far exceeds the diode shot noise for load resistances less than 100 megohms (see Figure 6). Thus in high frequency operation where low values of load resistance are required for high cut-off frequency, all PIN photodiodes contribute virtually no noise to the system (see Figures 6 and 7).

Ultra-fast operation is possible because the HP PIN photodiodes are capable of a response time less than one nanosecond. A significant advantage of the device is that this great speed of response is exhibited at relatively low reverse bias (−10 to −20 volts).

Because of its high sensitivity over a wide spectral range, unprecedented speed of response, unrivaled low-noise performance, and low capacitance, the HP PIN photodiodes are the most useful and versatile silicon photodiodes available.

NOTES:

1. Peak Pulse Power
   When exposing the diode to high level irradiance the following photocurrent limits must be observed:

   $$I_P\text{ (avg)} < \frac{0.1}{E_P}$$

   and

   $$I_P\text{ (peak)} < 500\text{ mA} \quad \text{or}$$

   $$< \frac{1000\text{ Amps}}{t(\mu\text{sec})} \quad \text{or}$$

   $$< \frac{I_p\text{ (avg)}}{ft}$$

   whichever of the above three conditions is least.
   I_P—photocurrent
   E_P—supply voltage
   t—pulse duration
   f—pulse repetition rate
2. Current Responsivity
   Response of the photodiode to a uniform field of irradiance H, parallel to the polar axis is given by

OPTICAL CHARACTERISTICS AT 25°C

Characteristics		Irradiance Response at 770 nm (1) (RA)	Sensitive Area (A)	Junction Diameter		Speed of Response	Detectivity (D*)	Noise Equivalent Power (NEP)
Units		μA/mW/cm²	cm²	Inches	mm	nsec	cm Hz$^{1/2}$/watt	W Hz$^{-1/2}$
Test Conditions		V = −20 R_L = 1 MΩ				V = −20 R_L = 50Ω	(0.8, 100, 6) (λ, f, Δf)	(0.8, 100, 6) (λ, f, Δf)
	Min.						0.9×10^{12}	
5082-4203	Typ.	1.0	2×10^{-3}	0.020	0,508	<1		
	Max.							5.1×10^{-14}
	Min.						4.1×10^{12}	
5082-4204	Typ.	1.0	2×10^{-3}	0.020	0,508	<1		
	Max.							1.2×10^{-14}
	Min.						3.95×10^{12} (2)	
5082-4205	Typ.	1.5 (2)	3×10^{-3} (2)	0.010	0,254	<1		
	Max.							1.4×10^{-14}
	Min.						2.5×10^{12}	
5082-4207	Typ.	4.0	8×10^{-3}	0.040	1,016	<1		
	Max.							3.6×10^{-14}
	Min.						0.57×10^{12}	
5082-4220	Typ.	1.0	2×10^{-3}	0.020	0,508	<1		
	Max.							8×10^{-14}

NOTES:

(1) Response at 770 nm may be described as a RESPONSIVITY, R ≈ 0.5 μA/μW corresponding to a quantum efficiency, η ≈ 0.75 electron/photon (see Figure 1).
(2) Specification includes lens effect.

I = (RA) × H for 770 nm. The response from a field not parallel to the axis can be found by multiplying (RA) by a normalizing factor obtained from the radiation pattern at the angle in question. For example, the multiplying factor for the 5082-4207 with irradiance H, at an angle of 40° from the polar axis is 0.8. If $H = 1\ mW/cm^2$, then I = k × (RA) × H; I = 0.8 × 4.0 × 1 = 3.2 μamps.

To obtain the response at a wavelength other than 770 nm, the relative spectral response must be considered. Referring to the spectral response curve, Figure 1, obtain response, X, at the wavelength desired. Then the ratio of the response at the desired wavelength to response at 770 nm is given by:

$$\text{Ratio} = \frac{X}{0.5}$$

Multiplying this ratio by the current response at 770 nm will give the current response at the desired wavelength.

3. 5082-4205 Mounting Recommendations
   a. The 5082-4205 is intended to be soldered to a printed circuit board having a thickness of from 0.020 to 0.060 inch (0,051 to 0,152 cm).
   b. Soldering temperature should be controlled so that at no time does the case temperature approach 280°C. The lowest solder melting point in the device is 280°C (gold-tin eutectic). If this temperature is approached, the solder will soften, and the lens may fall off. Lead-tin solder is recommended for mounting the package, and should be applied with a small soldering iron, for the shortest possible time, to avoid the temperature approaching 280°C.
   c. Contact to the lens end should be made by soldering to one or both of the tabs provided. Care should be exercised to prevent solder from coming in contact with the lens.
   d. If printed circuit board mounting is not convenient, wire leads may be soldered or welded to the devices using the precautions noted above.

ELECTRICAL CHARACTERISTICS AT 25°C							MAXIMUM RATINGS		
Junction Capacitance		Capacitance to Shield		Dark Current		Series Resistance	Steady Reverse Voltage	Peak Inverse Voltage	Power Dissipation
pF	pF	pF	pF	pA	pA	Ω	Volts	Volts	mW
$V_R = -10$ V	$V_R = -25$ V	$V_R = -10$ V	$V_R = -25$ V	$V_R = -10$ V	$V_R = -25$ V				25°C
	1.5		2						
					2000	50	50	200	100
2.0		2							
				600		50	20	200	100
0.7		*							
				150		50	50	200	50
5.5		2							
				2500		50	20	200	100
2.0		*							
					5000	50	50	200	100

* Not isolated from header.

Exceeding the peak inverse voltage may cause permanent damage to the diode. Forward current is harmless to the diode, within the power dissipation limit. For optimum performance, the diode should be reverse biased at between 5 and 20 volts.

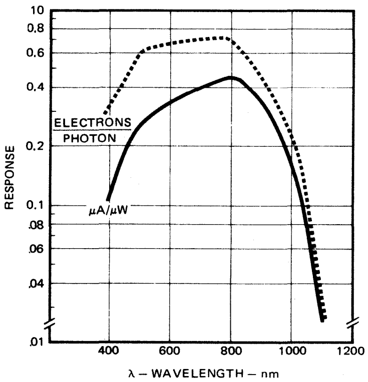


Figure 1. Spectral response.

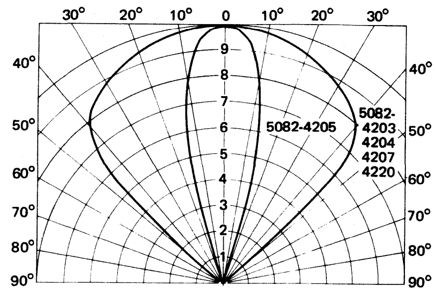


Figure 2. Relative directional sensitivity of the PIN Photodiodes.

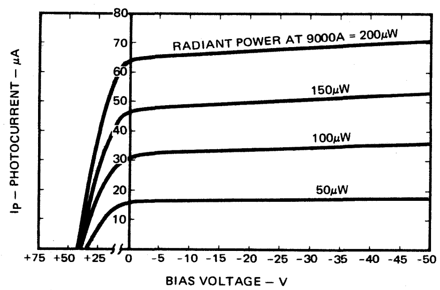


Figure 3. Typical output characteristics at λ = 900 nm.

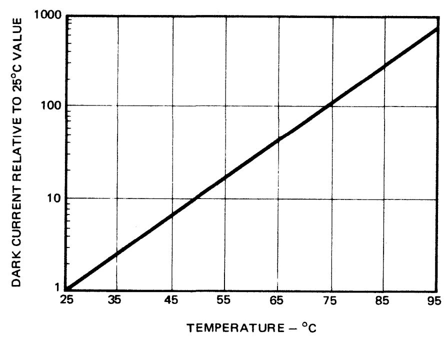


Figure 4. Dark current at —10 V bias vs. temperature.

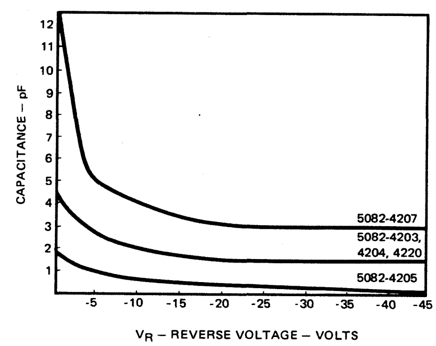


Figure 5. Typical capacitance variation with applied voltage.

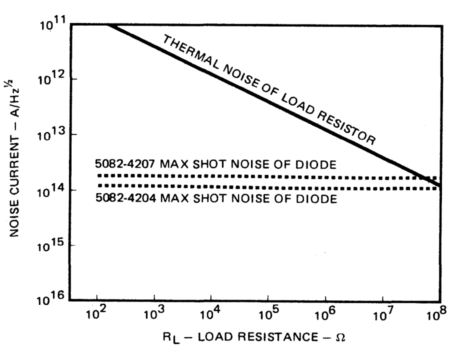


Figure 6. Noise vs. load resistance.

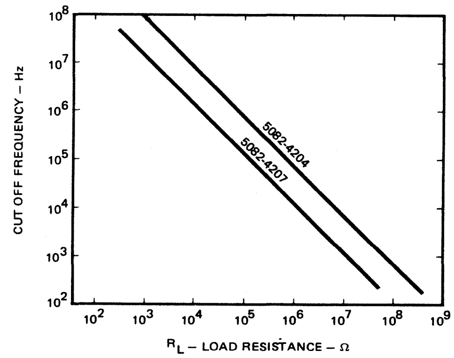


Figure 7. Photodiode cut-off frequency vs. load resistance (C = 2 pF).

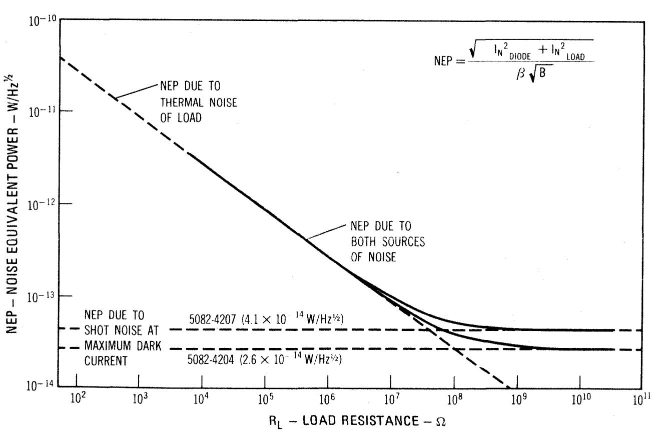


Figure 8. Noise equivalent power vs. load resistance.

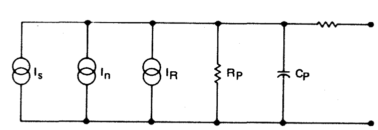


Figure 9.

i_s = Signal current ≈ 0.5 μA/μW × P input

i_n = Shot noise current

< 1.2 × 10^{-14} amps/$Hz^{1/2}$ (5082-4204)

< 4 × 10^{-14} amps/$Hz^{1/2}$ (5082-4207)

I_R = Dark current

< 600 × 10^{-12} amps at —10 V dc (5082-4204)

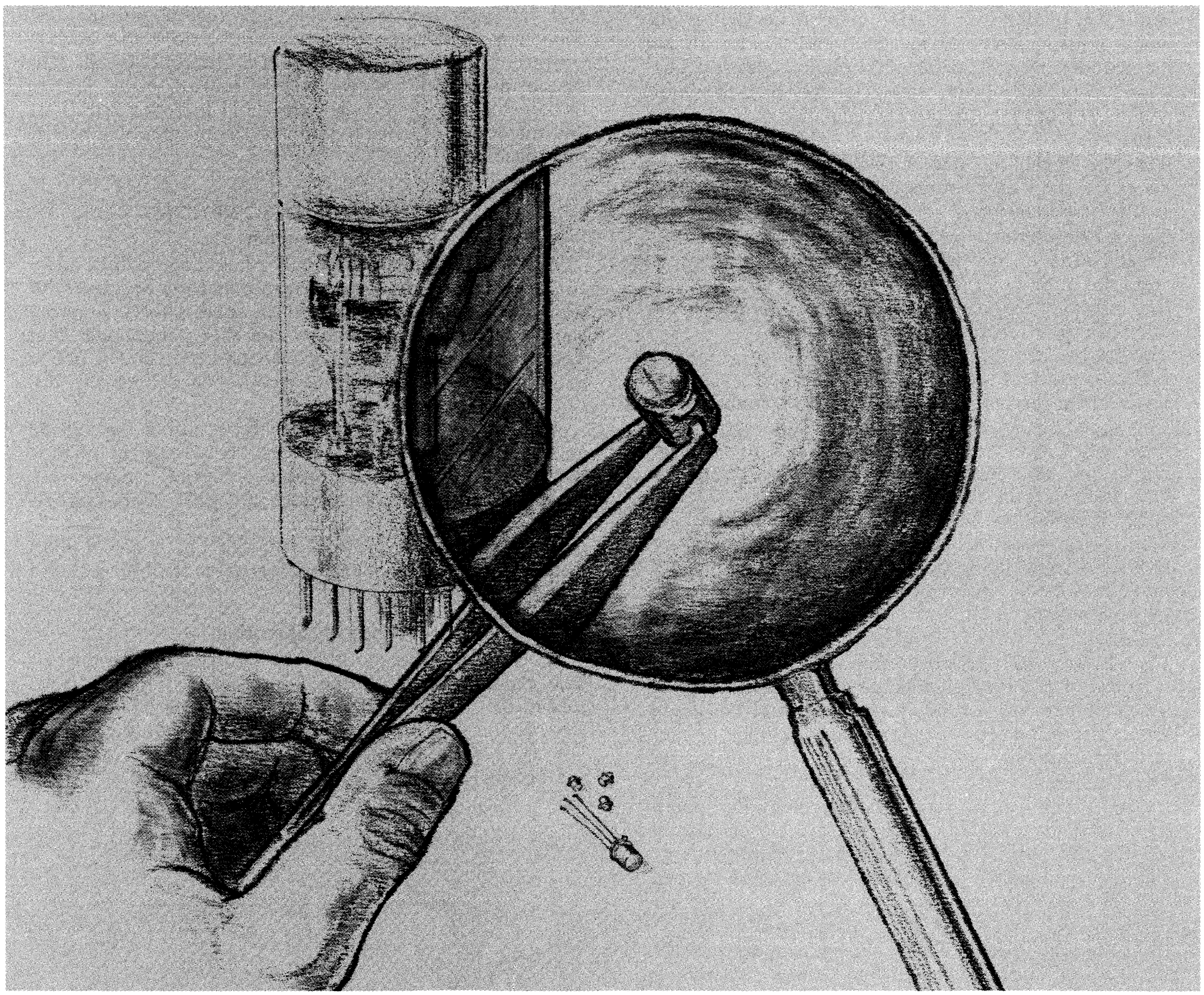
< 2500 × 10^{-12} amps at —10 V dc (5082-4207)

R_P = 10^{11} Ω

R_S = < 50 Ω

APPLICATION NOTE 915

THRESHOLD DETECTION OF VISIBLE AND INFRARED RADIATION WITH PIN PHOTODIODES



HEWLETT PACKARD

Traditionally, the detection and demodulation of extremely low level optical signals has been performed with multiplier phototubes. Because of this tradition, solid-state photodetectors are often overlooked even though they have a number of clear functional advantages and in some applications provide superior performance as well. Some of these advantages are summarized below and become even more apparent in the following discussion.

ADVANTAGES OF PIN PHOTODIODES VERSUS MULTIPLIER PHOTOTUBES

1. Size and weight:
   PIN photodiodes are approximately three orders of magnitude smaller and lighter. This greatly simplifies and reduces the cost of mounting.
2. Power Supply:
   Multiplier phototubes require more than 1000 volts, which must be precisely regulated and divided among the dynodes. By comparison, PIN photodiodes and associated amplifiers operate stably on less than 20 volts, which does not require precise regulation.
3. Cost:
   The cost, including that of the necessary amplifier, is lower for the PIN photodiode because of lower power supply requirements.
4. Spectral Response:
   Broad skirts of the PIN photodiode make it useful from the ultra-violet, through the visible, and well into the infrared region. This exceeds the range of any other device of comparable sensitivity.
5. Sensitivity:
   Noise equivalent power of the PIN photodiode is lower than that of any other type of photodetector. The signal levels are extremely low, however, and to achieve low level performance they require a high gain, high input resistance amplifier. Multiplier phototubes have built-in gain and do not require additional low-noise amplification. Moreover, the high input resistance needed for sensitive performance precludes fast response, whereas the response time of multiplier phototubes may be in the nanosecond region even in the sensitive mode.
6. Stability:
   The characteristics of noise, responsivity, and spectral response of the PIN photodiode are not dependent on time, temperature, or other environmental considerations. The same conditions may be hazardous to multiplier phototubes.
7. Overloading:
   In the presence of excessive signal, multiplier phototubes of comparable sensitivity are capable of destroying themselves as a result of excessive output current. The PIN photodiode is unaffected by exposure to room light or even direct sunlight.
8. Ruggedness:
   PIN photodiodes can tolerate exposure to extreme levels of shock and vibration. Typical shock capability is 1500 G's for 0.5 millisecond.
9. Magnetic Fields:
   Multiplier phototube gain is affected by fields as small as one gauss. If the interfering field is fluctuating, the output will be modulated by it. The PIN photodiode is insensitive to magnetic fields.
10. Precision:
    The responsivity of the PIN photodiode is inherently precise and repeatable. Within a given type, the characteristics agree (from unit to unit) within plus or minus 0.1 decade. Responsivity of multiplier phototubes may vary over more than a decade from one unit to another.
11. Sensitive Area:
    The small sensitive area of the PIN photodiode makes it unnecessary to establish an aperture which may be required for some applications. However, in some applications good optical alignment is imposed by the small area.

PIN PHOTODIODE DETECTORS

At the present time a variety of different types of solid-state photodetectors are available. Of these, the Silicon PIN Photodiode has the broadest applicability and is the subject of this note. The PIN photodiode's main advantages are: broad spectral response, a wide dynamic range, high speed, and extremely low noise. With appropriate terminal circuits it is well suited for many applications that require converting an optical signal to an electrical signal. The present discussion, however, will be limited to the description of the PIN photodiode's threshold detection sensitivity and the design of suitable terminal circuits that will realize this capability.

PHOTODIODE DESCRIPTION

Construction

A brief description of the PIN photodiode will be helpful in understanding its performance and the principles for designing appropriate circuits to be used with it. Figure 1 shows a typical construction of the PIN photodiode. This figure is for the purpose of explanation only and is not to scale. The relative proportions have been deliberately distorted for the sake of clarity.

The PIN structure is produced by diffusion through an oxide (S_iO_2) mask which also serves to protect the surface. Since most metals are very opaque to optical radiation, especially at infrared wavelengths, the gold contact is deposited only around the perimeter of the P-layer, and the gold contact pattern provides for lead attachment a short distance away from the junction region, so the lead is not in the light path.

Mode of Operation

When a photon is absorbed by the silicon it produces a hole and an electron. If the absorption of the photon occurs in the I-layer, as shown in Figure 1, the hole and the electron are separated by the electric field in the I-layer. For the highest quantum conversion efficiency (electrons per photon) it is desirable to have the P-layer as thin as

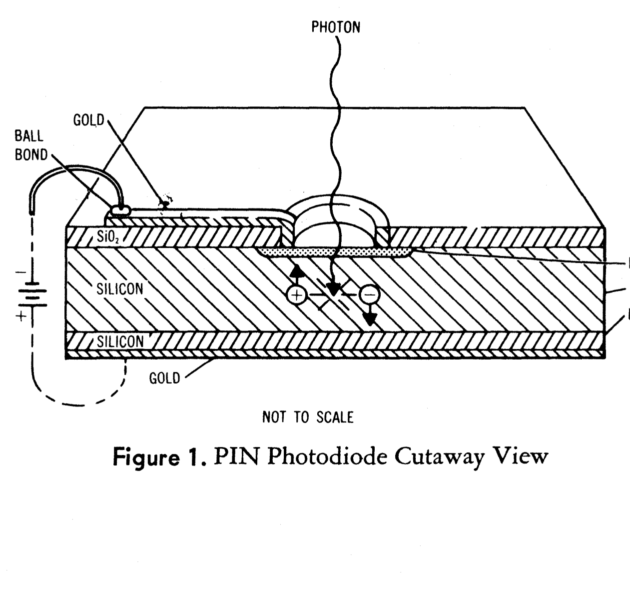


Figure 1. PIN Photodiode Cutaway View

possible and the I-layer as thick as possible. The thickness of the P-layer also determines the value of the parasitic series resistance (R_S in Figure 2). The thinner the P-layer the higher the R_S. Since R_S affects high frequency performance there is therefore a design trade-off between quantum efficiency and bandwidth. Once the trade-off is settled, the desired thickness is then controlled during the diffusion process. The effective thickness of the I-layer is controlled partly by the manufacturing diffusion process and partly by the magnitude of the electric field applied to the diode—the higher the field, the thicker will be the effective I-layer. It is therefore desirable to operate the diode with an external reverse bias, as shown in Figure 2. As the reverse bias voltage is increased from zero, there are three beneficial effects: hole and electron transit time decreases; conversion efficiency increases slightly; and most importantly, the capacitance decreases sharply with bias up to about ten volts and continues to decrease slightly up to about twenty volts reverse bias.

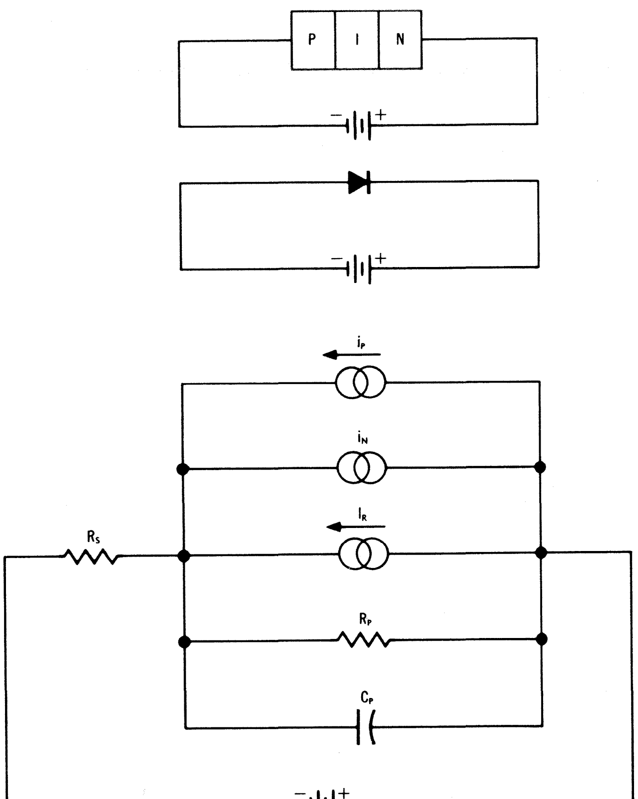


Figure 2. PIN Photodiode Schematic Symbol, and Equivalent Circuit

In the presence of optical signals there is a slight modulation of the shunt conductance as the presence of photon-produced holes and electrons in the I-layer modulate its conductivity. This effect can be quite significant at very high levels of illumination since the I-layer may become saturated, resulting in a decrease in quantum efficiency and an increase in rise time. Saturation can be prevented by applying a very high reverse bias voltage (up to 200 volts). However, such a high voltage, applied over a long period of time, may cause a degradation of the diode's leakage properties. Since our present concern is with threshold performance, reverse bias voltages greater than twenty volts need not be considered.

Equivalent Circuit

When properly biased, the PIN photodiode can be accurately represented by the equivalent circuit shown in Figure 2. Here i_p is the external current resulting when the diode is illuminated. It has a time constant of 10 picoseconds and a value of approximately 0.5 amp per watt of input at a wavelength of 8000 angstroms (800 nanometers). This corresponds to a quantum efficiency of 75%, that is, 0.75 electrons per photon. The quantum efficiency is constant from 500 nanometers to 800 nanometers (5,000 Å to 8,000 Å).

i_N is the noise current of the PIN photodiode. Since the diode is reverse biased, the shot noise formula is applicable, so that the noise current can be computed from:

$$\frac{i_N^2}{B} = 2qI_{dc} \qquad (1)$$

where B = system output bandwidth, Hz
q = electron charge, 1.6×10^{-19} coulombs
I_{dc} = dc current, Amp.

In the case of the photodiode, I_{dc} is simply the dark current, I_R, which has a value determined by the construction and dimensions of the particular diode type. Maximum values are: 100 picoamps for HPA 4204, 150 picoamps for HPA 4205 and 2 nanoamps for HPA 4203.

Shunt resistance, R_p, is very large, being usually greater than 10 gigaohms (10,000 megohms), and its noise current may therefore be neglected. Shunt capacitance, C_p, has a value from two to five picofarads, depending upon the diode type and reverse bias. For high frequency operation it is important to minimize C_p because the cutoff frequency is determined by:

$$f_c = \frac{1}{2\pi R_s C_p} \qquad (2)$$

Although our present concern is with low frequency threshold operation, there is another reason for minimizing C_p. This will be discussed later, when circuit design principles are presented.

Performance

Threshold performance can and has been specified in a number of different ways. The most commonly understood and usable expression takes the form of a noise equivalent input signal. This is the input signal which produces an output signal level that is equal in value to the noise level that is present when no input signal is applied. The noise equivalent input in watts is called Noise Equivalent Power (NEP) and is defined by:

$$\text{NEP} = \frac{\text{NOISE CURRENT (amps per root hertz)}}{\text{CURRENT RESPONSIVITY (amps per watt)}} \qquad (3)$$

which has the units of watts per root hertz. Devices for photo-detection could then be compared on the basis of NEP. The lower the NEP the more sensitive is the device.

Another method of defining threshold sensitivity is on the basis of signal-to-noise ratio for given input signal power levels. Taking a power level of one picowatt, for example, the signal-to-noise ratio at the output can be obtained from:

$$\text{SNR} = \frac{\text{RESPONSIVITY} \left(\frac{\text{amps}}{\text{watts}}\right) \times \text{INPUT (watts)}}{\text{NOISE CURRENT (amps)}} \qquad (4)$$

This is a ratio of currents. To express it in dB we would take twenty times its log to base ten, even though the expression converts linearly to a power ratio. This is because the devices respond *linearly* to input *power.*

Figure 3 shows spectral sensitivity characteristics of several PIN photodiodes and multiplier phototubes. Sensitivity is given in terms of SNR and NEP. The latter is in terms of dBm. Several interesting features are evident in Figure 3. Although the quantum efficiency for PIN photodiodes is constant from 500 to 800 nanometers, the sensitivity curve is not. This is due to the fact that the energy per quantum (photon) of radiant energy varies with wavelength.

The curves for the three different PIN photodiodes also show the dependence of sensitivity on leakage current. Here the highest sensitivity is obtained with the HPA 4204 which has a maximum leakage current of 100 picoamps. Next is the HPA 4205 with 150 picoamps and finally the HPA 4203 with maximum leakage of 2 nanoamps. The three curves are in effect displaced by the magnitude of the noise current difference because quantum efficiency is equal for all. These curves also show the inherent broad response of PIN photodiodes with respect to multiplier phototubes. Therefore, the power responsivity of the PIN photodiode has a corresponding slope. Notice how the inherently broad response of silicon, enhanced by the thick I-layer construction, extends the range of useful performance over the response ranges of two types of photocathodes.

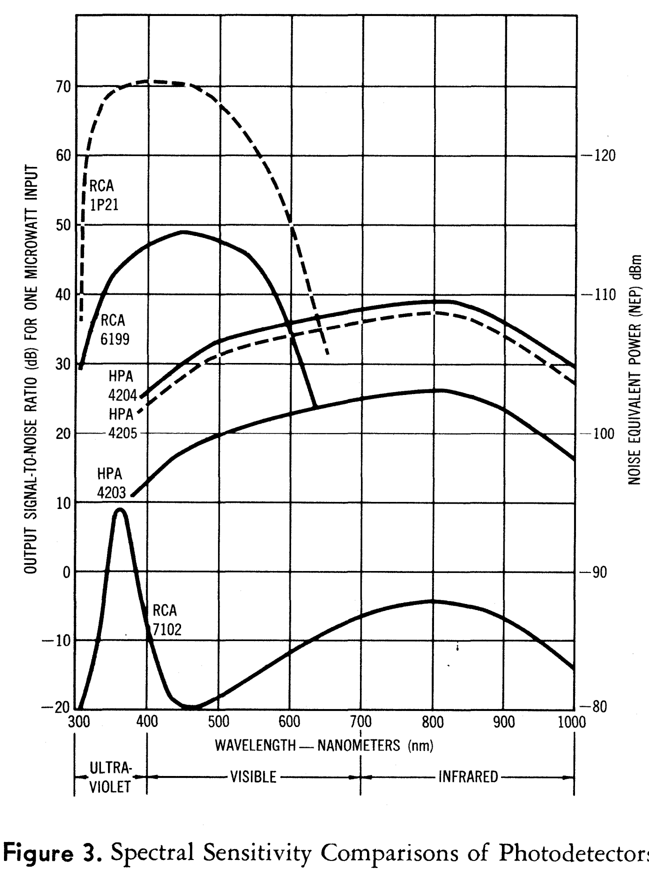


Figure 3. Spectral Sensitivity Comparisons of Photodetectors

Although the threshold sensitivity of multiplier phototubes is superior in the visible region, nevertheless for many applications the advantage is not significant enough to outweigh the disadvantages of generally unstable and temperature-sensitive gain, large size and weight, and the need of very high and stable power supply voltages. On the other hand, the superior red and infrared threshold performance of the PIN photodiode does not necessarily mean it is better in any application, because one must take into account its small sensitive area and low signal levels. Realization of the performance capability described in Figure 3 also requires fairly careful attention to the design of the terminal circuits into which the PIN photodiode operates.

TERMINAL CIRCUIT DESIGN PRINCIPLES

The design of the terminal amplifier must consider the usual design objectives of low noise, broad band, wide dynamic range, etc. In addition, there are two fundamental considerations which are dictated by the PIN photodiode:

1. High Reverse Voltage:
   The diode must be operated at ten to twenty volts of reverse bias to reduce shunt capacitance.
2. High Input Resistance:
   This is a fundamental consideration in the sensitivity/rise time trade-off.

The effects of reverse voltage on capacitance have been discussed earlier. However, the effect is sufficiently important to deserve a re-emphasis here.

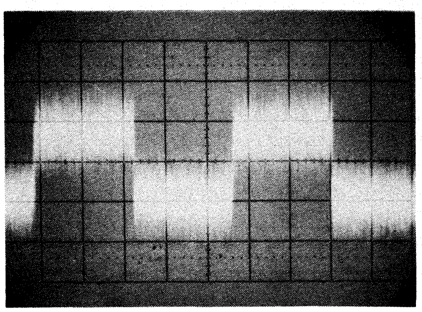
A high input resistance is necessary in order to maintain a high signal-to-noise ratio. Since the output signal from the photodiode is a current, and its own internal noise is represented by a current, it is appropriate to represent the noise of the terminal amplifier as an equivalent noise current at the input. The smallest value of resistor which may be connected to the input is then limited by its noise current according to the formula for thermal noise:

$$\frac{i_N^2\ (\text{thermal})}{B} = \frac{4kT}{R} \qquad (5)$$

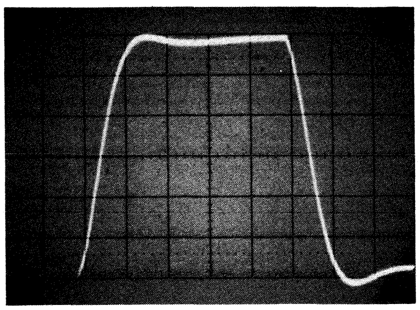
By comparing eq(1), relating diode noise current to leakage current, with eq(5), relating resistor noise current to its resistance value, it is clear that there is some value of resistance below which the NEP of the system, i.e., threshold sensitivity, would be degraded at the rate of 5 dB per decade of decreasing resistance. For example, in the case of the HPA 4203, assuming a maximum leakage current of 2 nanoamps, the value of resistance should be greater than 25 megohms, to avoid degrading the threshold sensitivity.

TRANSISTOR AMPLIFIER

In addition to keeping the input noise current low by using large values of input resistance, it is also important to keep other sources of noise in the amplifier at a minimum. Using ordinary transistors (PNP or NPN) it is not possible to approach the ultimate sensitivity of which the PIN photodiode alone is capable, even when low-noise transistors, such as the 2N2484, are used. However, in those applications where it is possible to sacrifice sensitivity for simplicity, transistors may be used. A typical transistor circuit is shown in Figure 4. With this circuit, a sensitivity corresponding to an NEP of — 95 dBm was obtained. In this case, Q1 was operated at the lowest possible collector current which would still give adequate gain. A high loop gain was desired in order to compensate, with negative feedback, for the long open-loop rise time produced by the high input resistance. A resistance higher than 10 megohms was not necessary here, since the transistor itself sets the fundamental noise limitation. A PNP transistor was selected for Q2 in order to balance out most of the base-to-emitter voltage of Q1, so that the output would tend to be near zero without any zero adjustment. A slight zero adjustment, provided by R2 and R3,



400 μV/cm × 1 msec/cm



VERTICAL: (UNSPECIFIED)
HORIZONTAL: 20 μsec/cm

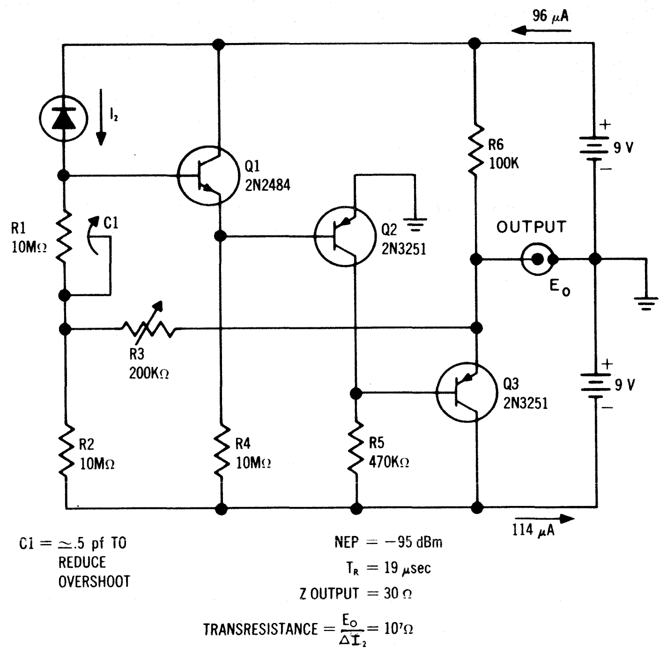


Figure 4. Transistor Photodiode Amplifier Schematic

gives the necessary range without appreciably attenuating the feedback current. As the photocurrent, I_2, increases, the amplifier causes the voltage at the emitter of Q3 to decrease, which causes a current in R1 to flow out of the node (base of Q1) into which I_2 flows.

LEAD NETWORK COMPENSATION

Negative feedback is not the only way to compensate for the low cutoff frequency imposed by high input resistance. The important thing is to preserve the signal-to-noise ratio. An ordinary lead network at the output can be used to compensate for the gain slope of the photodiode/amplifier system having low cutoff frequency. An example of such a network is shown in Figure 5. A word of caution here: There may be considerable attenuation in the lead network, but the signal level must not be allowed to fall so low that the signal-to-noise ratio is affected. This scheme therefore requires a higher amplifier gain, A, than there is loss in the lead network. Since the use of negative feedback will tend to stabilize the gain of the system, it is ordinarily preferred over lead-network compensation.

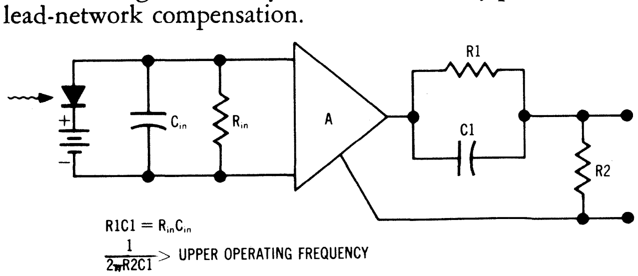


Figure 5. Lead-Network Compensation for Low Cutoff Frequency

When ultimate sensitivity is required, it is necessary to use an electrometer type of amplifier, but even with such an amplifier a careful design technique must be used. The principle involved in this technique is to simply represent all sources of noise in the amplifier as equivalent currents at the input. Noise sources which produce a constant output voltage with frequency, such as field-effect transistor channel noise and thermal noise, acquire an $(f)^{+1}$ spectral shape when they are referred to the input as equivalent currents because they are multiplied by the input susceptance. By plotting the asymptotes of noise current per root hertz from various sources in the amplifier, a profile of the variation with frequency of the signal-to-noise ratio can be obtained. Such a plot of asymptotes is shown in Figure 6. The limits within which the photodiode noise dominates are abundantly clear.

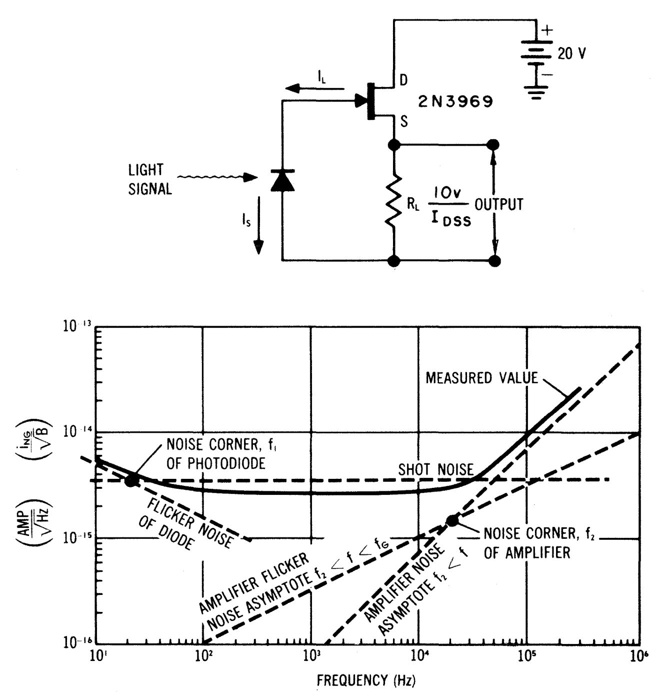
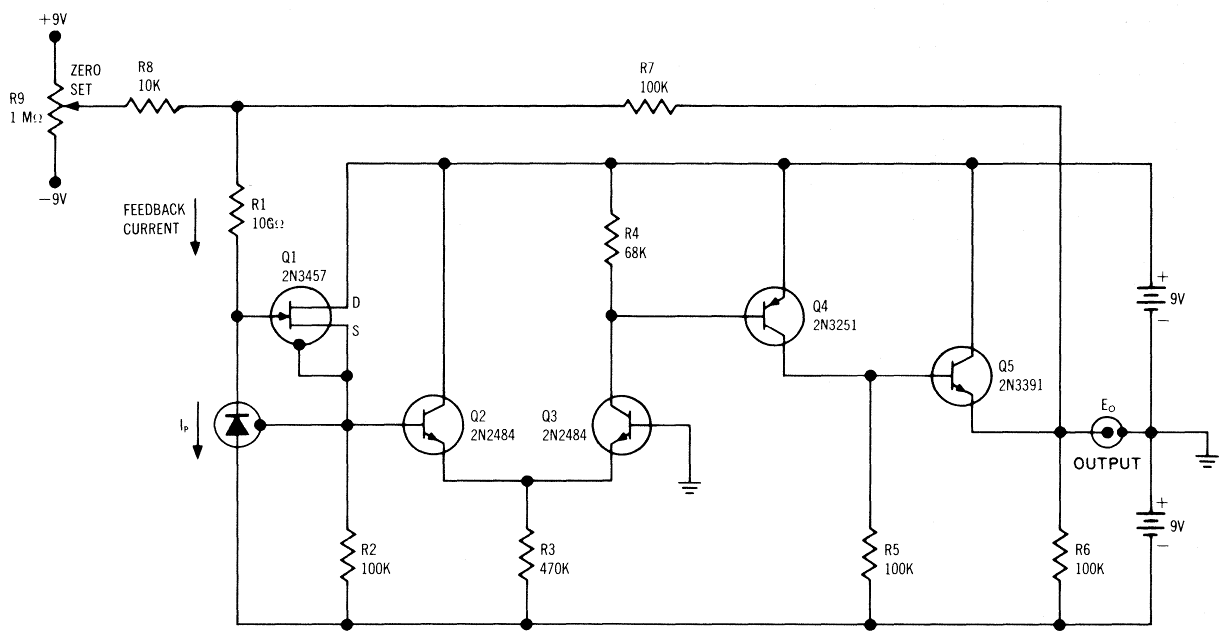


Figure 6. Calculated and Measured Noise Current Referred to Gate of Field Effect Transistor

A diffused-channel FET is selected for this application because its noise properties are much better than the MOS type. Suggested FET types are the 2N3457 and 2N3969 from Amelco Semiconductors, or similar low-noise field effect transistors.

In providing compensation for the low cutoff frequency, the circuit given in Figure 7 illustrates the feedback technique. A resistor of 10 gigaohms (10,000 megohms) was used for the feedback resistance, although the noise calculation indicated that 1.0 gigaohm (1000 megohms) would have been large enough. This is because the actual noise current is often actually less than the shot noise computed from leakage current, and leakage current is typically less than the specified maximum.

The FET is operated as a source follower, rather than a voltage amplifier, to avoid multiplication of the gate-to-drain capacitance. The source load resistance was selected so that, with I_{DSS} flowing in the channel, the source voltage would be near ground. A differential amplifier (Q2 and Q3) referred to ground was chosen rather than a single stage in order to keep the impedance at the source of Q1 as high as possible, and thus keep the signal-to-noise ratio high. Q4 provides the phase reversal needed for negative feedback and Q5 is added to keep the output impedance low.



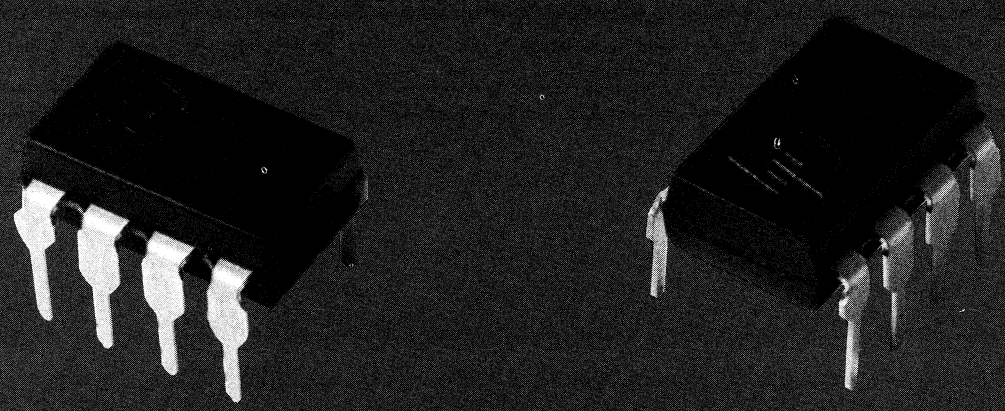
AMPL. TRANSRESISTANCE $= \frac{\Delta E_O}{\Delta I_P} = 1.5 \times 10^{10} \frac{\text{Volt}}{\text{Amp.}} = \frac{15 \text{ Volts}}{\text{per nA}}$

BANDWIDTH = 100 Hz

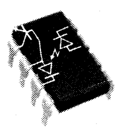
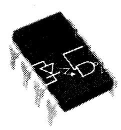
NOISE EQUIV. INPUT $= 42 \times 10^{-15} \frac{\text{watts}}{\sqrt{\text{Hz}}}$ / $= -104$ dBm — AT 800 NANOMETERS; $= 2.1 \times 10^{-5}$ FOOT-CANDLES AT 555 NANOMETERS

Figure 7. FET Amplifier with Current Feedback to Improve Bandwidth

Isolators



Isolators

Device		Application	Typical Signal Handling Capabilities @ 25°C	Typical Current Transfer Ratio @ 25°C	Input to Output Voltage	Page No.
	5082-4350	High Speed Analog and Digital Signal Conditioning (For further information, see Application Note 939, page 23.)	5 MHz	11%	2500V	15
	5082-4351			22%		
	5082-4352			15-22%[1]		
	5082-4360	TTL Compatible High Speed Digital Data Transmission (For further information, see Application Note 939, page 23.)	20M Bits	600%		19

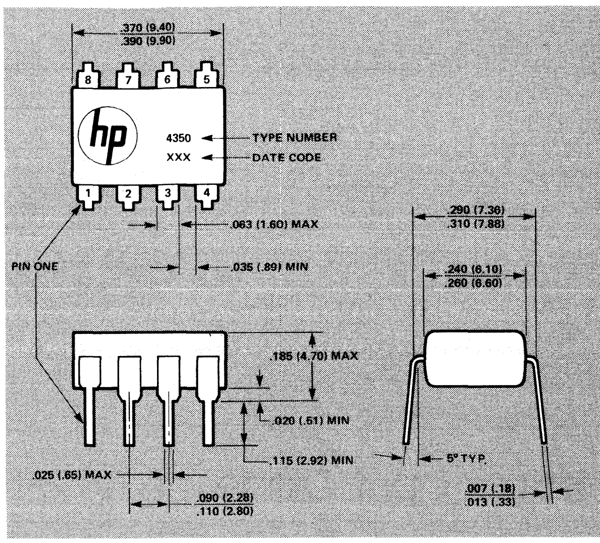
NOTE 1: The 5082-4352 Current Transfer Ratio Specification is guaranteed to be 15% minimum and 22% maximum.

HEWLETT hp PACKARD
COMPONENTS

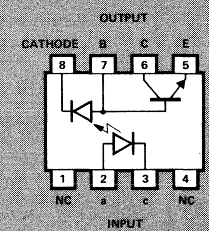
HIGH SPEED OPTICALLY COUPLED ISOLATORS 5082-4350 5082-4351 5082-4352

Features

- SHORT PROPAGATION DELAY – 225ns
- TTL COMPATIBLE – Input and Output
- HIGH COMMON MODE REJECTION – 30V at 2MHz
- HIGH DC INSULATION VOLTAGE – 2500V



PIN CONNECTION DIAGRAM



	PIN	FUNCTION
INPUT	1	NC
	2	Anode
	3	Cathode
	4	NC
OUTPUT	5	Emitter
	6	Collector
	7	Base
	8	Cathode

Description

The 5082-4350 Series combines a Light Emitting Input Diode, optically coupled with a p-n photodiode, driving a high speed transistor. The GaAsP input diode emits photons in proportion to its forward current. These photons are received by the p-n photodiode detector and amplified by the high speed transistor. Optical coupling provides a high degree of DC as well as AC isolation. This unique design maximizes the gain bandwidth product, permitting direct coupling to TTL loads at TTL speeds without additional buffers, triggers, etc.

The 5082-4350 Series consists of three devices:

1. The 5082-4350 - designed for general purpose isolation applications.
2. The 5082-4351 - can be used where high gain is required.
3. The 5082-4352 - intended for critical gain control situations.

Applications

These devices are suitable for high speed digital and analog line receivers, floating power supply feedback networks, replacements for pulse transformers and mechanical relays. They can also be used to eliminate ground loop currents between modules of a system.

Absolute Maximum Ratings

Storage Temperature .... –55°C to 125°C

Operating Temperature .... –55°C to 100°C

Lead Solder Temperature .... 260°C for 10 Sec.

Input Diode (T_A = 25°C)
- Forward DC Current .... 20mA (see Note 1)
- Forward Peak Current 40mA
- Reverse Voltage 5V
- Power Dissipation .... 35mW (see Note 2)

Output Detector/Transistor (T_A = 25°C)
- Collector DC Current 8mA
- Collector Peak Current 16mA
- Emitter to Base Voltage 5V
- Collector to Emitter Voltage 15V
- Detector Cathode to Base Voltage 15V
- Power Dissipation .... 100mW (see Note 3)

Insulation Voltage (Input—Output) 2500V

Transfer Characteristics - Coupled at T_A=25°C

Parameter	Symbol	5082-4350 Min.	5082-4350 Typ.	5082-4350 Max.	5082-4351 Min.	5082-4351 Typ.	5082-4351 Max.	5082-4352 Min.	5082-4352 Typ.	5082-4352 Max.	Units	Test Conditions	Notes
Current Transfer Ratio	CTR	7	11		15	22		15		22	%	I_F = 16mA, V_{CE} = 5V	4

Electrical Characteristics - Coupled at $T_A = 25°C$

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Notes
Insulation Voltage (Input to Output)	V_{I-O}	2500			V		
Resistance (Input to Output)	R_{I-O}	10^{12}			Ω	V_{I-O} = 500V	
Capacitance (Input to Output)	C_{I-O}		0.6	0.8	pF	f = 1MHz	
Collector-Emitter Saturation Voltage	V_{CE} (sat)		0.2	0.4	V	I_F = 16 mA	
Rise and Fall Time	t_r, t_f		350	500	ns	I_F = 16mA, V_{CE} = 5V R_L = 1kΩ (see Fig. 5)	5, 14
Delay Time	t_d		150		ns	I_F = 16mA, V_{CE} = 5V R_L = 1kΩ (see Fig. 5)	6
Storage Time	t_s		125		ns	I_F = 16mA, I_C = 1mA (see Fig. 5)	7
Propagation Delay	t_{pd}		225		ns	R_L = 1kΩ, V_{CE} = 5V, I_F = 16mA	8
Bandwidth	BW		4		MHz	V_{CE} = 5V, R_L = 100Ω, I_F = 12mA (see Fig. 4A)	9
Common Mode Rejection Voltage	CMRV		30		vrms	f = 2MHz, R_L = 4.7kΩ $V_{OUT\,max.}$ = 1.0 vrms (See Fig.7)	10

Electrical Characteristics - Input Diode at $T_A = 25°C$

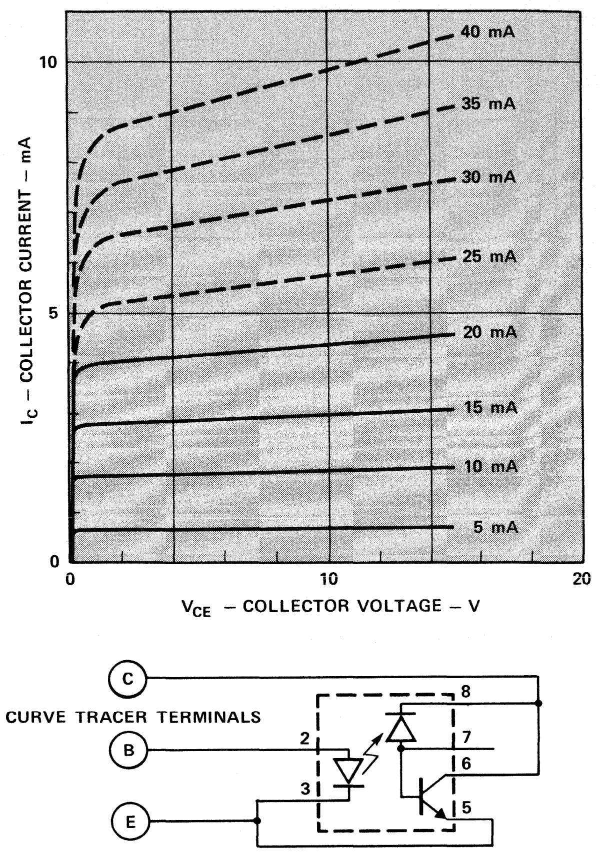
Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Notes
Forward Voltage	V_F		1.55	1.8	V	I_F = 16mA	11
Reverse Breakdown Voltage	BV_R	5			V	I_R = 10μA	
Capacitance	C_{IN}		40		pF	f = 1MHz, V = 0	

Electrical Characteristics - Diode/Transistor at $T_A = 25°C$

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Notes
DC Current Gain	h_{FE}	55	100			V_{CE} = 5V, I_C = 2mA	
Collector – Emitter Sustaining Voltage	LV_{CEO}	15	30		V	I_C = 100μA	12
Collector – Base Breakdown Voltage	BV_{CBO}	15	55		V	I_C = 10μA	
Photodiode Breakdown Voltage	BV_{DET}	15			V	I_D = 1μA	
Collector – Emitter Leakage Current	I_{CEX}		3	500	nA	V_{CE} = 5V	13
Collector – Base Capacitance	C_{CB}		0.4		pF	f = 1MHz, V_{CB} = 5V	14
Base – Emitter Capacitance	C_{BE}		2		pF	f = 1MHz, V_{BE} = 0	15
Photodiode Capacitance	C_{DET}		13		pF	f = 1MHz, V_{8-7} = 5V	

NOTES:

1. Derate Linearly from 50°C to 100°C free-air temperature at a rate of 0.4 mA/°C.
2. Derate Linearly from 50°C to 100°C free-air temperature at a rate of 0.7 mW/°C.
3. Derate Linearly from 50°C to 100°C free-air temperature at a rate of 2.0 mW/°C.
4. DC Current Transfer Ratio is defined as the ratio of Collector Current to the Forward Bias Input Current times 100%. This measurement is made with the cathode of the detector (pin 8) tied to the collector.
5. Rise Time is defined as the time required for the Collector Current to rise from 10% to 90% of peak value. Fall Time is defined as the time required for the current to decrease from 90% to 10% of peak value. This is measured with the cathode of the detector (pin 8) tied to the supply voltage.
6. Delay Time is defined as the time from the 50% point of the beginning of the input pulse to the time for the Collector Current to rise to 10% of peak value. This is measured with the cathode of the detector (pin 8) tied to the supply voltage.
7. Storage Time is defined as the time from the 50% point of the end of the input pulse to the time for the Collector Current to decrease by 10% of peak value. This is measured with the cathode of the detector (pin 8) tied to the supply voltage.
8. The Propagation Delay $t_{pd} = .5\,(t_d + .5t_r + t_s + .5t_f)$ – where t_d is the delay time, t_r is the rise time, t_s is the storage time and t_f is the fall time.
9. The frequency at which the AC Collector Current is 0.707 of the low frequency value.
10. The CMRV describes the device capability for rejecting common mode voltage - it is the input common mode voltage (rms) which produces less than one volt (rms) at the output under worst-case conditions. The test circuit is shown in Fig. 7, and when the appropriate curve of Input/Output Voltage Ratio is multiplied by V_{out} the CMRV is obtained vs. frequency. The equivalent common mode coupling capacitance is less than .07 pF.
11. At 16 mA V_F decreases with increasing temperature at the rate of 1.6 mV/°C.
12. Collector-Emitter Sustaining Voltage is measured with the base open and the detector cathode (pin 8) tied to the Collector.
13. Collector-Emitter Leakage current is measured with the base open and the detector cathode tied to the Collector. This adds the Detector Reverse Leakage multiplied by h_{FE} to the leakage of the transistor.
14. Rise time and frequency response are significantly degraded by the base-pin to collector-pin socket capacitance. The optimum speed of response is obtained with the base lead removed, or its socket pin removed. Capacitance measured with a guarded input bridge with pins 6 and 7 connected to bridge inputs and pin 5 connected to bridge ground.
15. Capacitance measured with a guarded input bridge with pins 5 and 7 connected to bridge inputs and pin 8 connected to bridge ground.



NOTE: DASHED CHARACTERISTICS ARE FOR PULSED OPERATION

Fig. 1. DC and Pulsed Transfer Characteristics

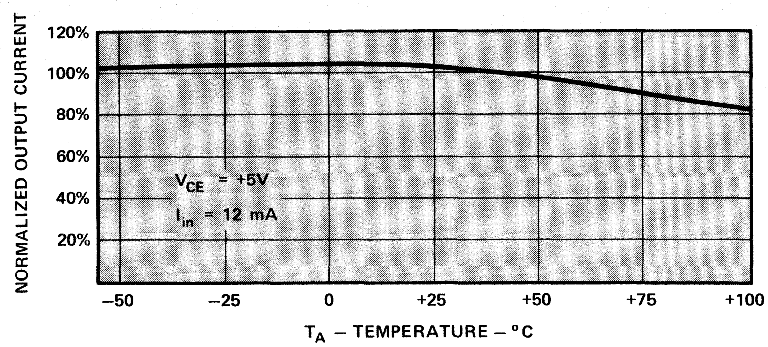


Fig. 2. Output Current vs. Temperature

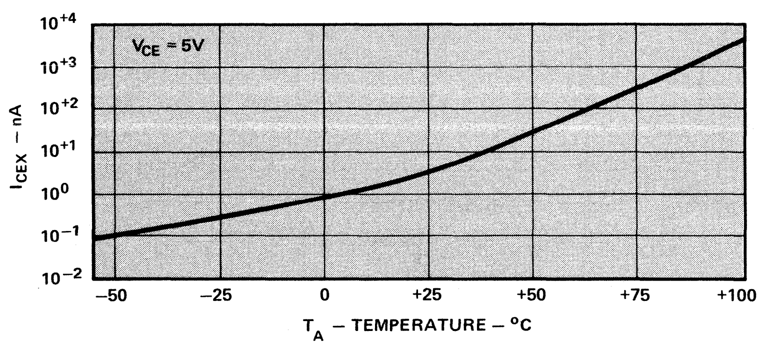


Fig. 3. Leakage Current (I_{CEX}) vs. Temperature

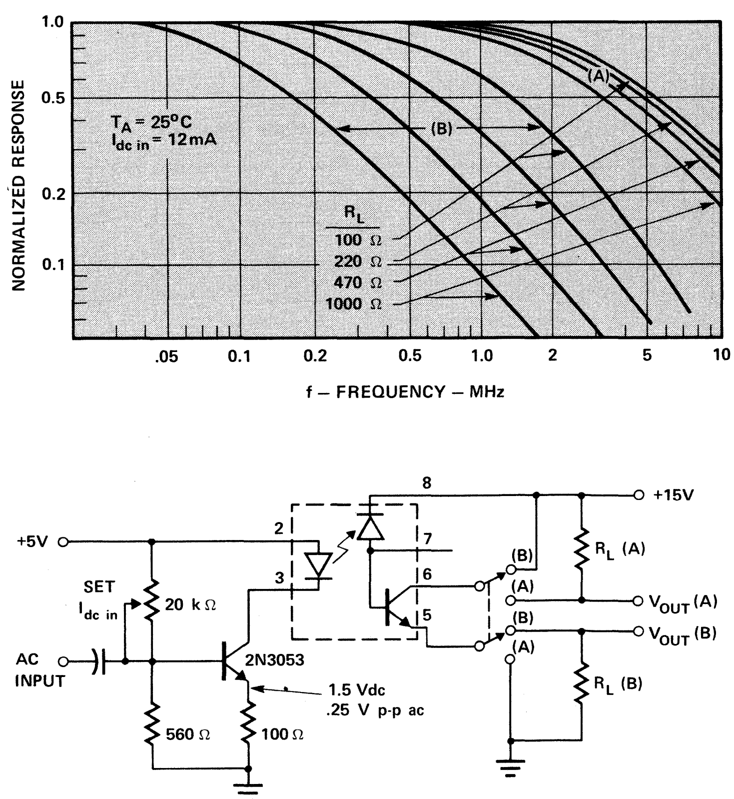
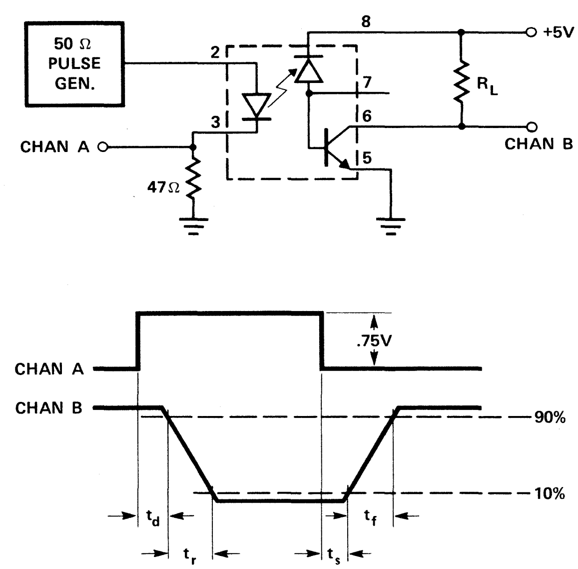


Fig. 4. Frequency Response–(A) High Frequency Mode
(B) Phototransistor Mode



R_L ohms	t_d nsec	t_r nsec	t_s* nsec	t_f nsec
100	150	150	5	170
220	150	180	10	190
470	150	200	20	210
1000	150	270	30	270

*t_s (STORAGE TIME) IS INSIGNIFICANT UNLESS DRIVEN TO SATURATION

Fig. 5. Pulse Response with 16 mA Pulse

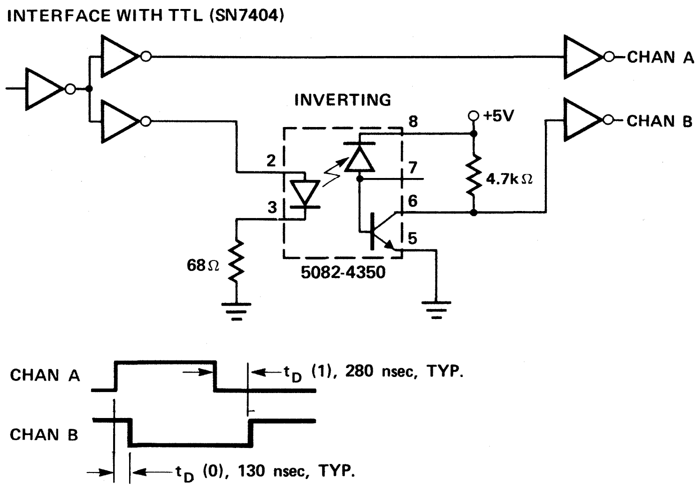


Fig. 6a. Inverting Logic Transmission with TTL Input/Output

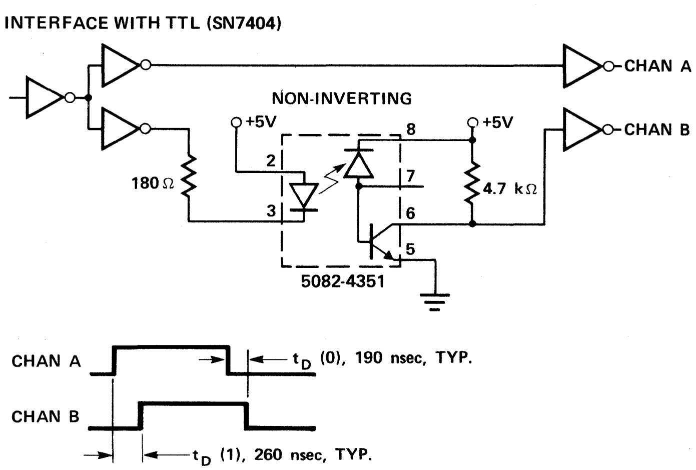
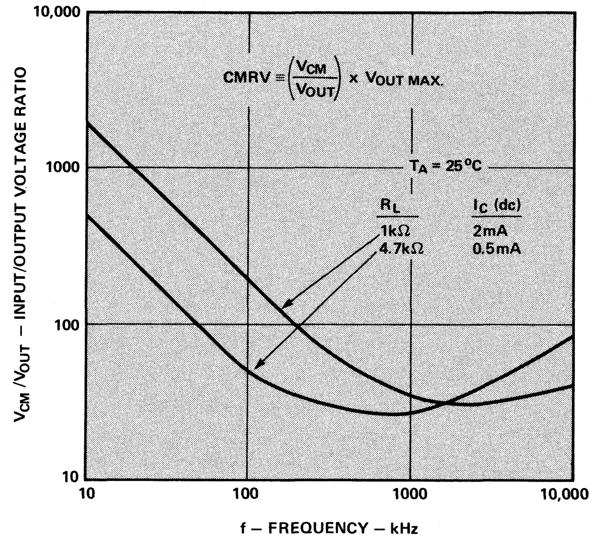


Fig. 6b. Non-Inverting Logic Transmission with TTL Input/Output



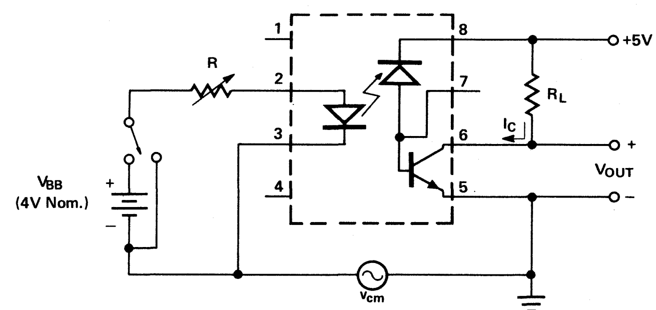
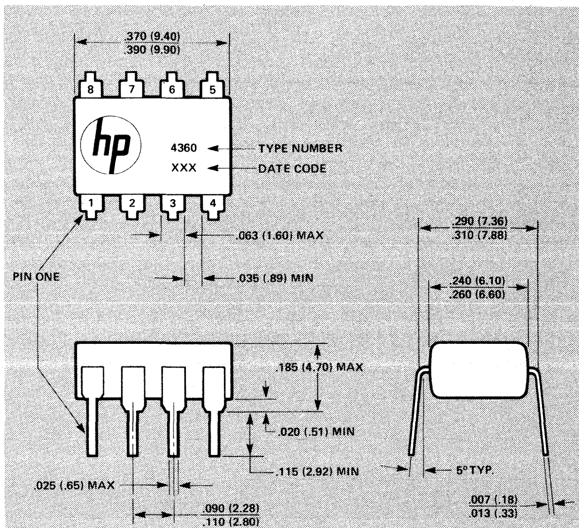


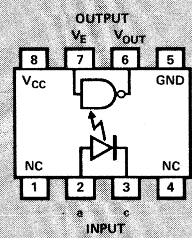
Fig. 7. Common Mode Rejection

HEWLETT PACKARD
COMPONENTS

DTL/TTL COMPATIBLE OPTICALLY ISOLATED GATE

5082-4360





TRUTH TABLE (Positive Logic)

Input*	Enable	Output
1	1	0
0	1	1
1	0	1
0	0	1

* See definition of terms for logic state.

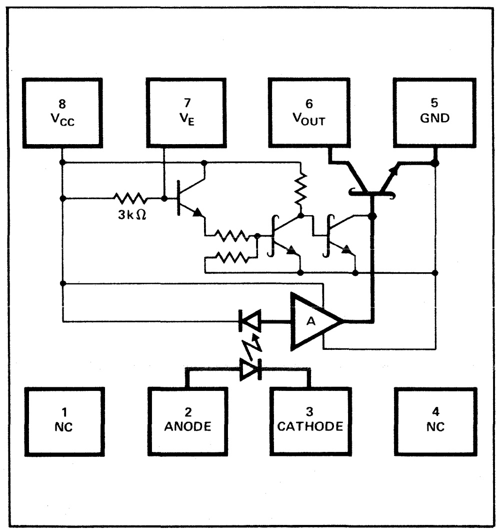


Figure 1. Schematic

Features

- DTL/TTL COMPATIBLE – 5V SUPPLY
- ULTRA HIGH SPEED – 20M BITS
- LOW INPUT CURRENT REQ. – 5mA
- HIGH COMMON MODE REJECTION – 20V @ 1MHz

Description/Applications

The 5082-4360 optical isolated gate combines a GaAsP diode that emits photons proportional to its forward current and a unique integrated detector. The photons are collected in the detector by a photo diode and then amplified by a high gain linear amplifier that drives a Schottky clamped open collector output transistor. The circuit is temperature, current and voltage compensated. The output circuit also has a DTL type enable input to provide strobing of the detector.

This unique isolator design provides maximum DC and AC circuit isolation between input and output while achieving DTL/TTL circuit compatibility. The isolator operational parameters are guaranteed from 0°C to 70°C, such that a minimum input current of 5 mA will sink an eight gate fan-out (13 mA) at the output with 5 volt V_{CC} applied to the detector. This isolation and coupling is achieved with a propagation delay of 63 nsec. The enable input provides gating of the detector with input sinking and sourcing requirements compatible with DTL/TTL interfacing and a propagation delay of 30 nsec typical.

The 5082-4360 can be used in high speed digital interface applications where common mode signals must be rejected; such as for a line receiver and digital programming of floating power supplies, motors, and other machine control systems. The elimination of ground loops can be accomplished between system interfaces such as a computer and a peripheral memory. The open collector in combination with the enable input provides capability for bussing, OR'ing, and strobing.

Recommended Operating Conditions

	Min.	Nom.	Max.	Units
Input Current - I_{in}	0		10	mA
Supply Voltage - V_{CC}	4.5	5.0	5.5	V
Fan-Out - N (TTL Load)			8	–
Operating Temperature Range - T_A	0	25	70	°C

Absolute Maximum Ratings

Storage Temperature . . . . –55°C to +125°C
Operating Temperature . . . . 0°C to +70°C
Lead Solder Temperature . . . . 260°C for 10 Sec.
Input Diode
  Forward DC Current 10mA
  Reverse Voltage 5V
Output - IC
  Supply Voltage - V_{CC} 7V
  Enable Input Voltage - V_E 5.5V
  (Not to exceed V_{CC} by more than 500mV)
  Output Collector Current - I_{OUT} 50mA
  Output Collector Power Dissipation 85mW
  Output Collector Voltage - V_{OUT} 7V
Insulation Voltage (Input-Output) 2500V

Electrical Characteristics
OVER RECOMMENDED TEMPERATURE ($T_A = 0°C - 70°C$)

Parameter	Min.	Typ.*	Max.	Units	Test Conditions	Figure	Note
$I_{in}(1)$: Logic (1) Input Current to Ensure Logic (0) Output	5			mA		3,4	–
$I_{in}(0)$: Logic (0) Input Current to Ensure Logic (1) Output			250	μA		3,4	–
$V_E(1)$: Logic (1) Enable Voltage	2.0			V		–	–
$V_E(0)$: Logic (0) Enable Voltage			0.8	V		–	–
$I_{out}(1)$: Logic (1) Output Current		50	250	μA	$V_{CC} = 5.5V$, $V_{out} = 5.5V$, $V_E = 2.0V$, $I_{in} = 250μA$	6	–
$V_{out}(0)$: Logic (0) Output Voltage		0.5	0.6	V	$V_{CC} = 5.5V$, $V_E = 2.0V$, $I_{in} = 5mA$, I_{out} (Sinking) = 13mA	5	–
$I_E(0)$: Logic (0) Enable Current		−1.6	−2.0	mA	$V_{CC} = 5.5V$, $V_E = 0.5V$	–	–
$I_E(1)$: Logic (1) Enable Current		−1.0		mA	$V_{CC} = 5.5V$, $V_E = 2.0V$	–	–
$I_{CC}(1)$: Logic (1) Supply Current		7	10	mA	$V_{CC} = 5.5V$, $V_E = 0.5V$, $I_{in} = 0$	–	–
$I_{CC}(0)$: Logic (0) Supply Current		13	18	mA	$V_{CC} = 5.5V$, $V_E = 0.5V$, $I_{in} = 10mA$	–	–

*All typical values are at $V_{CC} = 5V$, $T_A = 25°C$

Switching Characteristics at $T_A = 25°C$, $V_{CC} = 5V$

Parameter	Min.	Typ.	Max.	Units	Test Condtions	Figure	Note
$t_{pd}(1)$: Propagation Delay Time to Logical (1) Level		45	75	ns	$R_L = 350kΩ$, $C_L = 15pF$, $I_{in} = 7.5mA$	7,9	1
$t_{pd}(0)$: Propagation Delay Time to Logical (0) Level		45	75	ns	$R_L = 350Ω$, $C_L = 15pF$, $I_{in} = 7.5mA$	7,9	2
t_R, t_F: Output Rise, Fall Time (10-90%)		25		ns	$R_L = 350Ω$, $C_L = 15pF$, $I_{in} = 7.5mA$	–	–
$t_E(1)$: Propagation Delay Time of Enable from $V_E(1)$ to $V_E(0)$		25		ns	$R_L = 350Ω$, $C_L = 15pF$, $I_{in} = 7.5mA$ $V_E(1) = 2V$, $V_E(0) = 0.5V$	8	3
$t_E(0)$: Propagation Delay Time of Enable from $V_E(0)$ to $V_E(1)$		15		ns	$R_L = 350Ω$, $C_L = 15pF$, $I_{in} = 7.5mA$ $V_E(1) = 2V$, $V_E(0) = 0.5V$	8	4

Electrical Characteristics - Input-Output at $T_A = 25°C$

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Insulation Voltage (Input-Output)	BV_{I-O}	2500			V		–	5
Resistance (Input-Output)	R_{I-O}	10^{12}			Ω	$V_{I-O} = 500V$	–	5
Capacitance (Input-Output)	C_{I-O}		0.6	0.8	pF	f = 1MHz	–	5
Common Mode Rejection Voltage to Logical (0) Level	CMRV (1)		20		VAC p-p	f = 1MHz, $R_L = 350Ω$, V_{out}(min.) = 2V, $I_{in} = 0mA$	11	6
Common Mode Rejection Voltage to Logical (1) Level	CMRV (0)		60		VAC p-p	f = 1MHz, $R_L = 350Ω$, V_{out}(max.) = 0.6V, $I_{in} = 7.5mA$	11	6
Current Transfer Ratio	CTR		600		%	$I_{in} = 5.0mA$, $V_{CC} = 5V$, $R_L = 100Ω$	2	7

Electrical Characteristics - Input Diode at $T_A = 25°C$

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Forward Voltage	V_F	1.2	1.5	1.75	V	$I_{in} = 10mA$	4	8
Reverse Breakdown Voltage	V_{BR}	5			V	$I_R = 10μA$	–	–
Capacitance	C_{in}		25		pF	$V_F = 0$, f = 1MHz	–	–

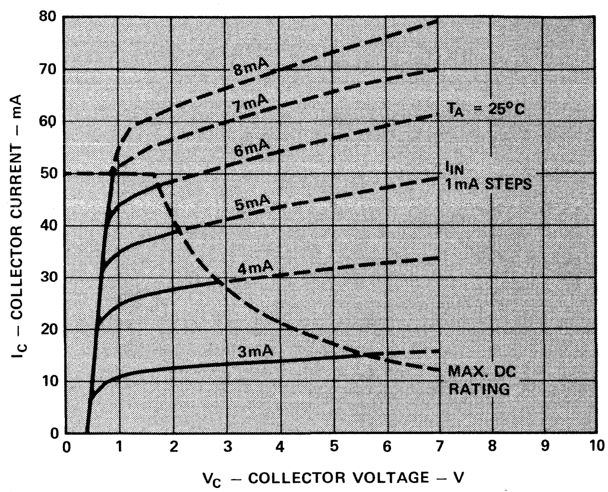
)perating Procedures and Definitions

ogic Convention. The 5082-4360 is defined in terms of ɔsitive logic.

ypassing. A ceramic capacitor (.01μF min.) should be con- ɜcted from pin 8 to pin 5. Its purpose is to stabilize the op- ·ation of the high gain linear amplifier. Failure to provide ıe bypassing may impair the switching properties.

olarities. All voltages are referenced to network ground ɔin 5). Current flowing toward a terminal is considered ositive.

nable Input. No external pull-up required for a logic (1), e., can be open circuit.



Note: Dashed characteristics — denote pulsed operation only.

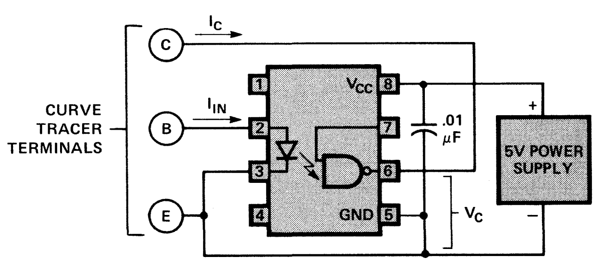


Figure 2. Isolator Collector Characteristics.

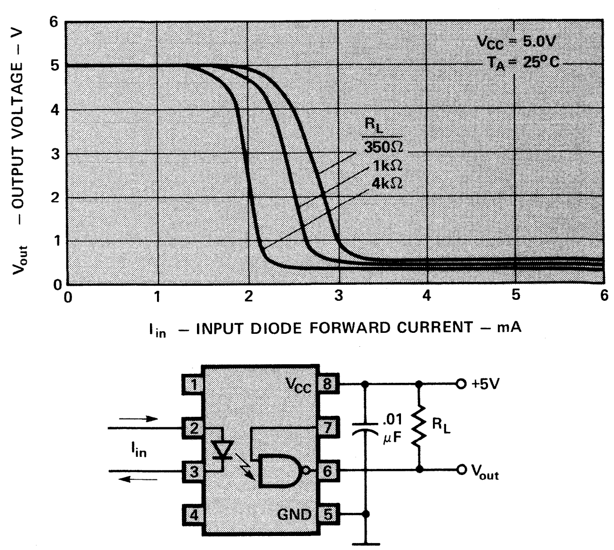


Figure 3. Input-Output Characteristics.

NOTES:

1. The $t_{pd}(1)$ propagation delay is measured from the 3.75 mA point on the trailing edge of the input pulse to the 1.5V point on the trailing edge of the output pulse.
2. The $t_{pd}(0)$ propagation delay is measured from the 3.75 mA point on the input pulse to the 1.5V point on the leading edge of the output pulse.
3. The $t_E(1)$ enable propagation delay is measured from the 1.5V point of the trailing edge of the input pulse to the 1.5V point on the trailing edge of the output pulse.
4. The $t_E(0)$ enable propagation delay is measured from the 1.5V point on the input pulse to the 1.5V point on the leading edge of the output pulse. The input diode is DC biased to 10 mA [$I_{in}(1)$].
5. Device considered a two terminal device: pins 2 and 3 shorted together, and pins 5, 6, 7, and 8 shorted together.
6. CMRV (1) is the max. tolerable common mode voltage to assure that the output will remain in a logic (1) state (i.e. $V_{out} > 2.0V$). CMRV (0) is the max. tolerable common mode voltage to assure that the output will remain in a logic (0) state (i.e. $V_{out} < 0.6V$).
7. DC Current Transfer Ratio is defined as the ratio of the output collector current to the forward bias input current times 100%.
8. At 10 mA V_F decreases with increasing temperature at the rate of 1.6 mV/°C.

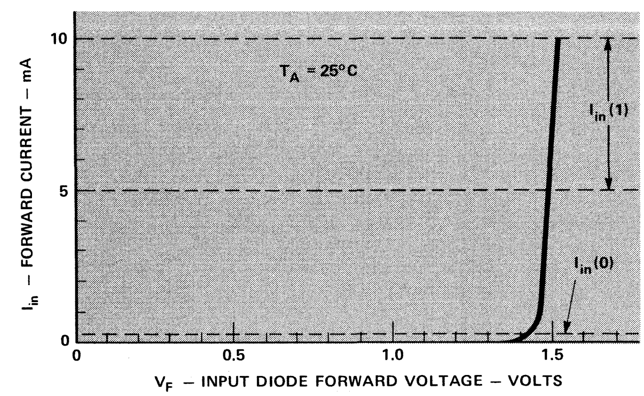


Figure 4. Input Diode Forward Characteristic.

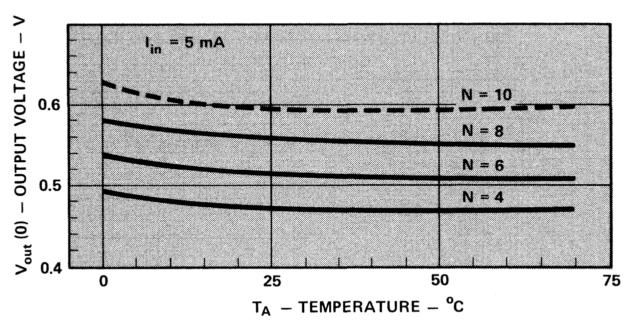


Figure 5. Output Voltage, $V_{OUT}(0)$ vs. Temperature and Fan-Out.

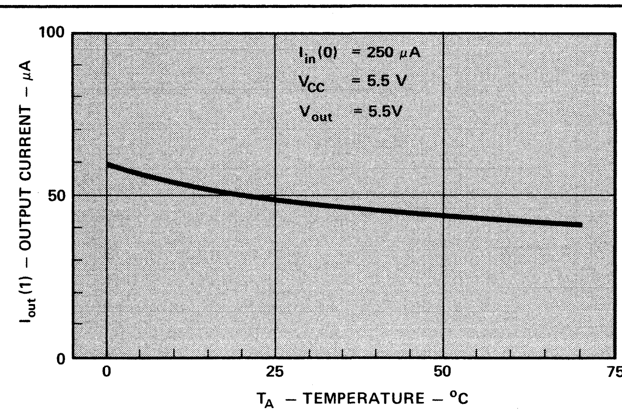


Figure 6. Output Current, $I_{OUT}(1)$ vs. Temperature (I_{in}=250μA).

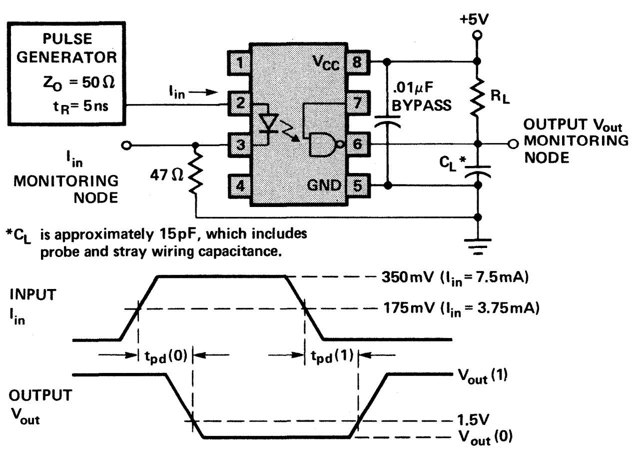


Figure 7. Test Circuit for $t_{pd}(0)$ and $t_{pd}(1)$.

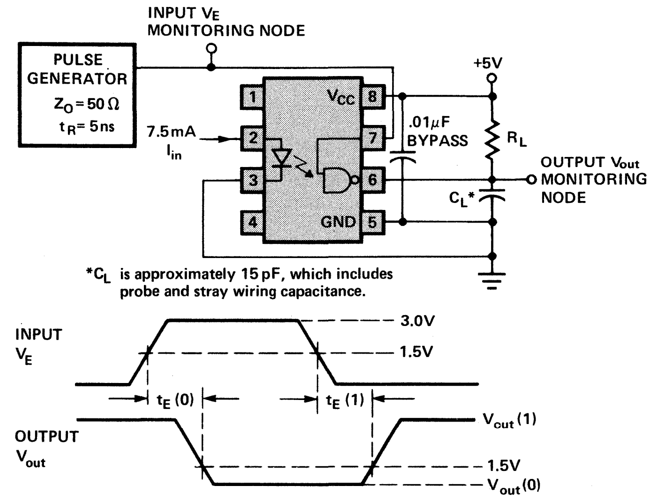


Figure 8. Test Circuit for $t_E(0)$ and $t_E(1)$.

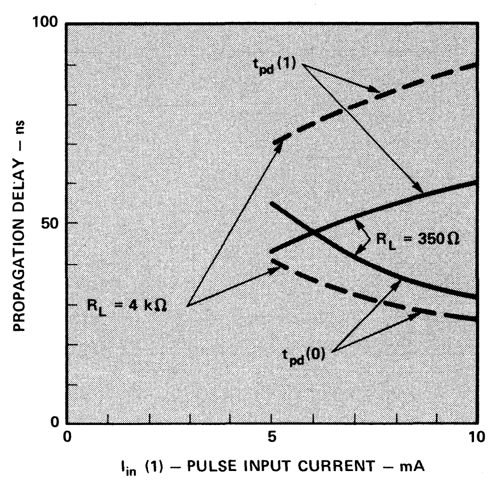


Figure 9. Propagation Delay, $t_{pd}(0)$ and $t_{pd}(1)$ vs. Input Pulse Current, $I_{in}(1)$.

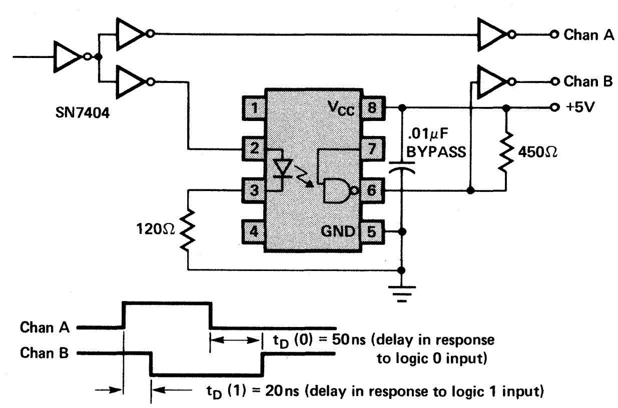


Figure 10. Response Delay Between TTL Gates.

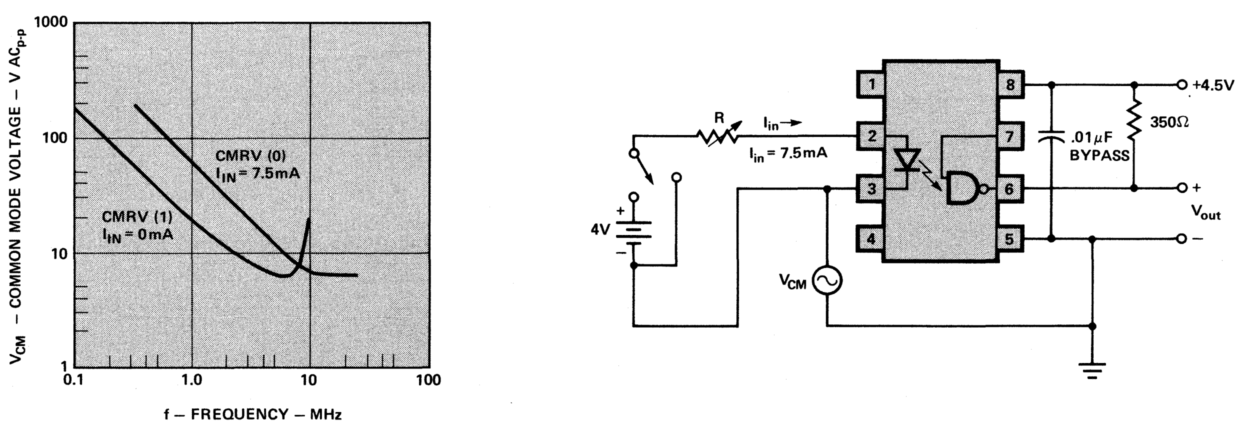
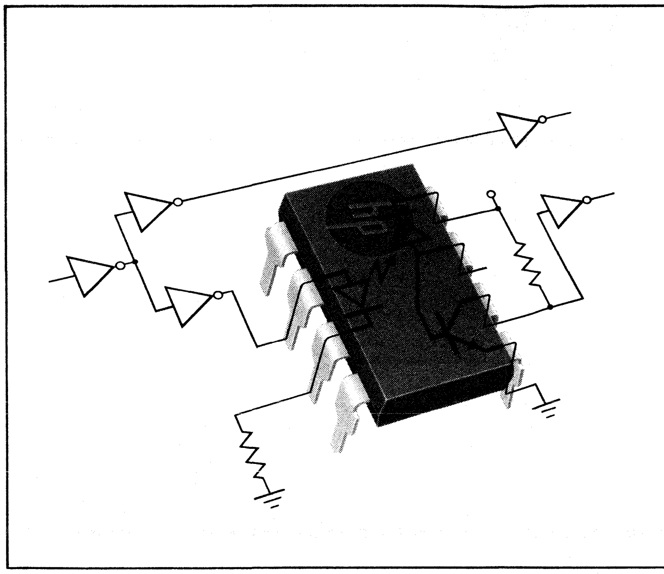
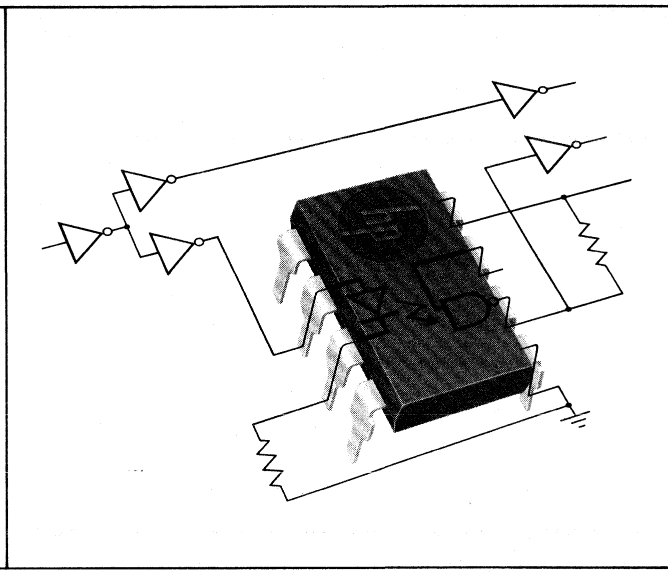


Figure 11. Typical Common Mode Rejection Characteristics/Circuit





HIGH SPEED OPTICALLY COUPLED ISOLATORS

HEWLETT hp PACKARD
COMPONENTS

INTRODUCTION

Often designers are faced with the problem of providing circuit isolation in order to prevent ground loops and common mode signals. Typical devices for doing this have been relays, transformers and line receivers. However, both relays and transformers are low speed devices, incompatible with modern logic circuits. Line receiver circuits are fast enough, but are limited to a common mode voltage of 3 volts. In addition, they do not protect very well against ground loop signals. Now Optically Coupled Isolators are available which solve most isolation problems.

The basic optically coupled isolator (Figure 1) consists of a Light Emitting Diode (LED) at the input, optically coupled to a photo-sensitive silicon detector at the output which is enclosed in the same package. This combination has semiconductor size, speed, and reliability, besides providing ac-dc isolation comparable to that of an electro-mechanical relay.

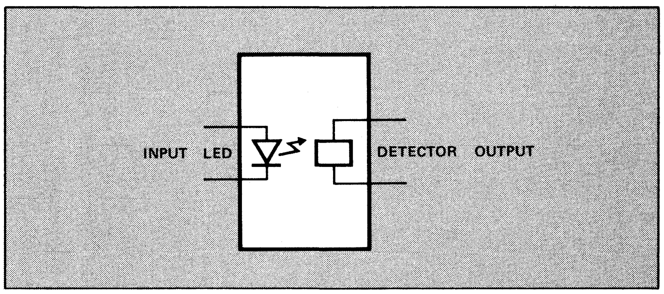


Figure 1. Basic Optically Coupled Isolator

A common type of optically coupled isolator (Figure 2) uses a phototransistor for a detector where the transistor provides the gain necessary to interface with logic circuits. The major problem with this phototransistor isolator is bandwidth, which limits the operating bandwidth to approximately 100kHz. This is due to the fact that both the detection of the photons and the amplification of the resulting photo current occur in the same physical structure in the phototransistor. The large feedback capacitance between the collector and the base is what essentially limits the phototransistor bandwidth.

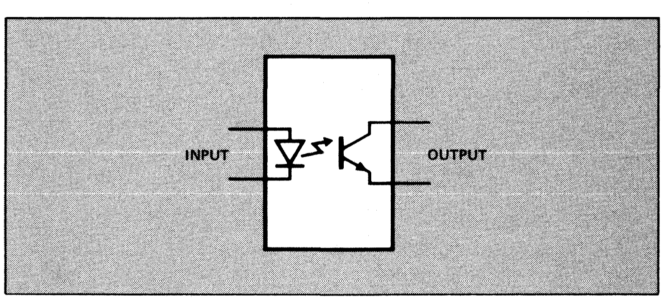
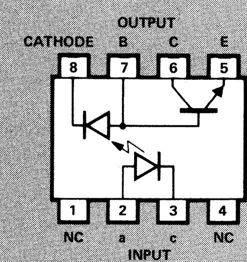


Figure 2. Phototransistor Isolator

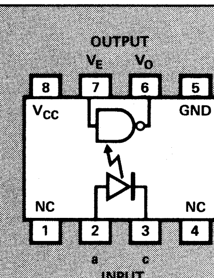
Hewlett-Packard's new 5082-4350 Series and 5082-4360 isolator designs greatly reduce this bandwidth limitation by proper optimization of the detector. The detector element is a monolithic structure, consisting of a photodiode, which collects the light; and a high frequency transistor, (Figure 3), or linear high speed amplifier (Figure 4), which amplifies the resultant photo current. Functional separation of the photodiode from the transistor or amplifier reduces feedback capacitance from approximately 15pF, which is typical for phototransistors to less than 1pF, thus making possible bandwidths up to 20MHz.



	PIN	FUNCTION
INPUT	1	NC
	2	Anode
	3	Cathode
	4	NC
OUTPUT	5	Emitter
	6	Collector
	7	Base
	8	Cathode

Figure 3. Diode/Transistor Isolator 5082-4350

The 5082-4350 is the Diode/Transistor type shown in Figure 3. The 5082-4360 is the IC-Gate type shown in Figure 4. Both are offered in a standard eight lead DIP package for ease of handling.



TRUTH TABLE (Positive Logic)

Input	Enable	Output
1	1	0
0	1	1
1	0	1
0	0	1

Figure 4. Diode/IC Isolator 5082-4360

This Application Note contains a description of these new high speed isolators, and discusses their applications in digital and analog systems.

5082-4350

The 5082-4350 (Figure 3) consists of a gallium arsenide phosphide input diode with a diode/transistor detector at the output. In addition to greater bandwidth, this series has many of the features of a phototransistor isolator (Table I), improved common mode rejection, easier interfacing with TTL/DTL circuits and tighter parameter control. This device can be connected in either of two ways. The first, a high frequency mode (Figure 5) in which the photodiode is separated from the collector of the gain transistor by the load resistor; or in the phototransistor mode (Figure 6) in which the photodiode is connected directly to the collector of the gain transistor. The 5082-4350 is suitable for both digital and/or analog applications.

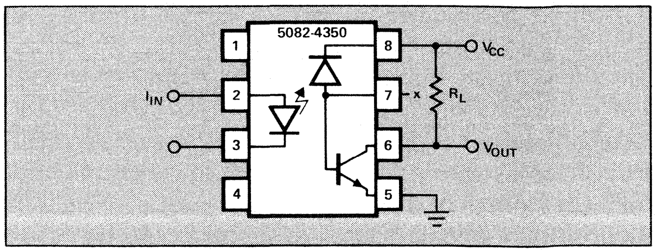


Figure 5. High Frequency Mode

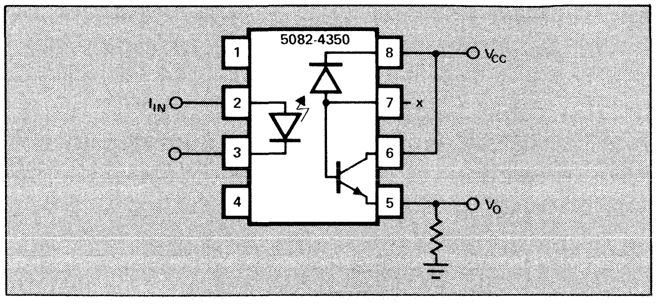


Figure 6. Phototransistor Mode

5082-4360

The 5082-4360 (Figure 4) consists of a gallium arsenide phosphide input diode and a monolithically integrated detector at the output. The detector consists of a photodiode followed by a linear amplifier which drives a Schottky clamped output transistor. This output circuit is temperature, voltage, and current compensated to be truly compatible with standard TTL and DTL circuits. It also has a DTL/TTL compatible strobing input; with logic '0' at the strobe input, the output is held at logic '1', regardless of input conditions at the gallium arsenide phosphide diode. The basic features of the 5082-4360 are given in Table I.

TABLE I.

ISOLATOR TYPES	BANDWIDTH BW	PROPAGATION DELAY	COMMON MODE REJECTION
5082-4360 (IC Compatible Optical Isolated Gate)	20 MHz (Data Rate)	60ns	10V/10MHz
5082-4350 (High Frequency Mode)	4 MHz	225ns	30V/1 MHz
5082-4350 (Phototransistor Mode)	500 kHz	1µs	30V/1 MHz
Phototransistor Types	100 kHz	6µs	3V/1 MHz

DIGITAL APPLICATIONS

TTL Interfacing

The 5082-4351 and -4360 isolators are TTL (also DTL) compatible at both the input and output. The 5082-4350 requires 16 mA of input current to sink the current from one standard TTL input, plus the current from the appropriate pull-up resistor. The 5082-4360 only requires 5 mA input current to sink 13 mA at the output – that is, it has 8-gate fan-out capability at 5 mA input.

Figure 7 shows the 5082-4351 interfacing with a TTL inverter. In Figure 7A, the inverting mode is shown, in which the input diode is 'off' when the output of the inverter is in the low state or the input diode is on and drawing 15 mA when the output of the inverter is in the high state. The output of the isolator is pulled up to 5 volts by the 4.7KΩ resistor when the input diode is off and will sink approximately 2.6 mA if the input diode is on (1.6 mA for the gate and 1.0 mA for the load resistor.) The typical delays which can be achieved with this circuit are also given in Figure 7A.

The non-inverting mode is considered in Figure 7B. This circuit is very similar to the inverting mode circuit, except for the input diode. The diode is now off when the inverter output is high and is drawing 16 mA when the inverter is low. The typical delays obtained with this circuit are also shown in Figure 7B.

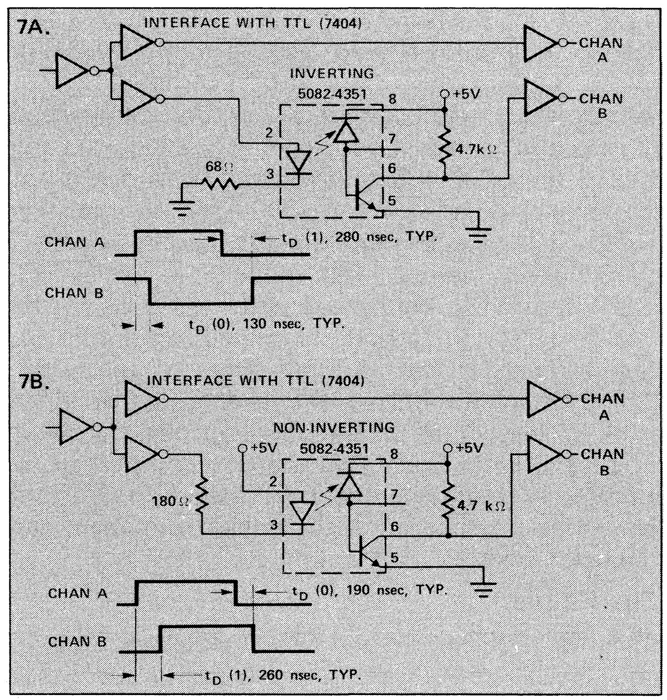


Figure 7. A. Inverting Logic Transmission with TTL Input/Output
B. Non-Inverting Logic Transmission with TTL Input/Output

The 5082-4360 interfacing with TTL inverters is demonstrated in Figure 8. The inverting mode achieves the best speed performance, with typical delays of 20 ns and 30 ns. The current limiting resistor in series with the input diode is 120Ω, allowing approximately 10 mA of current to flow in on the 'on' state. The output load resistor is only 350Ω, due to the greater sinking capability of the output transistor.

The input diode turn-on delay time of both 5082-4350 and -4360 is a function of the input charging time. This delay time is most easily improved by simply adding a capacitor in parallel with the input current limiting resistor and operating from a low impedance source. In general, the capacitor should be a low inductance type with a value for a time constant of 15 to 30ns with the current limiting resistor. If the current limiting resistor is 100Ω, the capacitor should be 150 to 300pF.

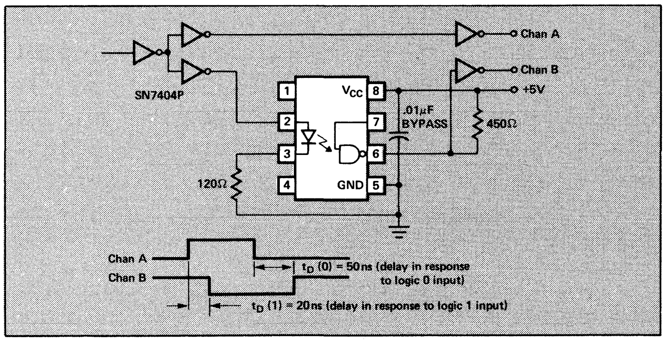


Figure 8. Response Delay Between TTL Gates

On the output side of the isolator, speed is enhanced by using the lowest possible value of pull-up resistance which is consistent with the current sinking capability of the isolator collector. The stray capacitance to ground should also be minimized. An output pull-up resistor is also recommended for both isolators to improve noise immunity and speed of response in moving to logic '1' output. In the case of the 5082-4350, the output transistor is not Schottky clamped as in the 5082-4360, so excessive storage delay can be eliminated by adding an exteranl Schottky clamp. This diode (e.g., HP 5082-2835) should be connected with its anode to the base (Pin 7), and cathode to the collector (Pin 6). Furthermore, if rise and fall times of the 5082-4350 are to be minimized, the feedback capacitance from collector to base of the output transistor should be minimized. This is best accomplished by completely removing the base lead (Pin 7) from the isolator package or the socket pin from the mounting board.

Line Receivers

Both the 5082-4350 and -4360 isolators may be used for line receivers, and are useful for either single-ended or balanced line applications. The turn-on voltage of the input diode establishes a threshold for the flow of current, thereby making the noise immunity higher than it would be for a linear line receiver. In many applications, this noise immunity is high enough that only a single-ended transmission line is required. For transmission over long distances or in very noisy environments, a balanced system should be used.

Figure 9 demonstrates the use of the 5082-4350 and -4360 as balanced line receivers, using two different types of line drivers. The resistor values were chosen in each case to match the line driver to the isolator line receiver. The line driver should be designed to supply more current than the isolator input diode requires; this permits the use of a shunt resistor at the receiving end for better impedance matching and improved noise immunity. To maintain a reasonable impedance match during the negative excursion when the isolator input diode is reversed biased, a diode having about the same turn-on voltage as the input diode should be connected in reverse polarity across the input diode. For this purpose two silicon diodes in series could be used, or one LED, such as the HP 5082-4403, or the input of another isolator to be driven at the same input current but with reverse logic. The circuits shown were tested using 300 feet of Belden No. 8777 cable. The delay was approximately 500ns for this cable length, and the rise and fall times were consistent with the results obtained in the previous section (TTL Interfacing) for the two isolator types.

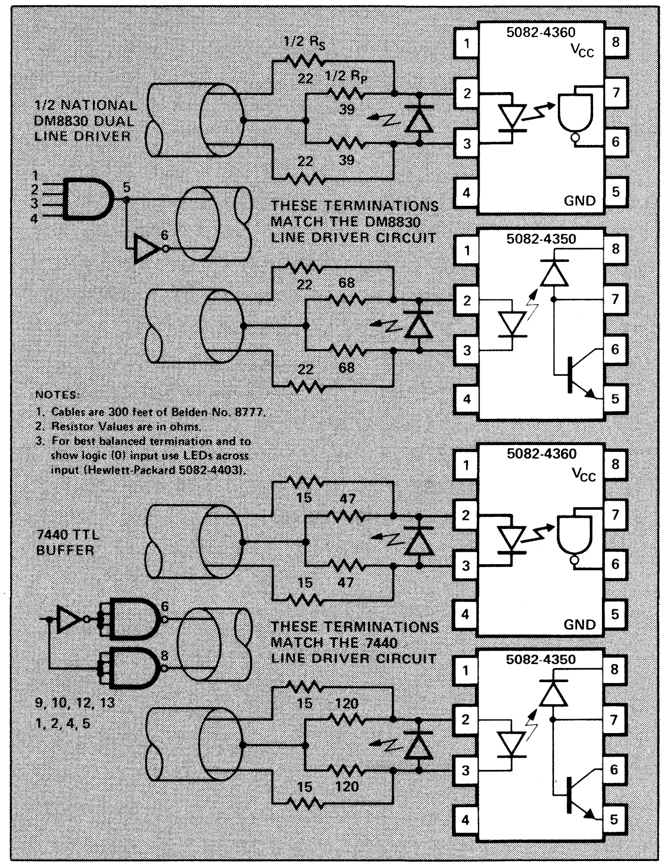


Figure 9. Typical Line Driver/Receiver System

Formulas for the terminating resistances are given in Table II.

TABLE II.

	BASICALLY	GIVEN R_O, I_L	GIVEN R_O, V_L	FOR BEST CMR
R_P	$\frac{V_D}{I_L - I_D}$	$\frac{V_D}{I_L - I_D}$	$R_O \left(\frac{V_D}{V_L - I_D R_O}\right)$	Connect ½ Rp from each side of isolator input to cable shield.
R_S	$\frac{V_L - V_D}{I_L}$	$R_O - \frac{V_D}{I_L}$	$R_O \left(1 - \frac{V_D}{V_L}\right)$	Connect ½ Rs in series from each line to input terminal of isolator.

R_O — line-to-line terminating resistor which gives least reflection.

V_L , I_L — line-to-line voltage and line current with R_O connected.

V_D , I_D — isolator input diode forward voltage and current.

Since they are open-collector, the outputs of the isolators may be "wired-OR" connected. It is also permissible to parallel IC isolator outputs with D/T isolator outputs, although if this is done, the fan-out of the wired-OR line is limited by the current-sinking capability of the D/T isolator.

Circuit Board Layout

5082-4350

When using the 5082-4350, the layout for either prototype breadboard or finished product is not especially critical because the gain is not high enough to support spurious oscillation. However, if high speed of response is important, it is well to avoid using a socket because the rise and fall times can be degraded by capacitive coupling to the base (Pin 7), especially from the collector (Pin 6). If the base is not to be connected (e.g., for negative feedback) the best performance is obtained by clipping the base lead (Pin 7) from the package before installation. Next best, if the device is soldered into the board or if an in-the-board socket (e.g., Berg Minisert) is used, leave a vacant, unmetallized hole in the board for Pin 7. If neither of these techniques can be used, then leave a hole in the board and/or remove the socket pin from position 7.

5082-4360

More careful attention is required for the 5082-4360 circuit layout due to the high gain employed in its internal amplifier. Power Supply lead lengths (Pins 5 and 8) are particularly important as their inductance provides an impedance across which a positive feedback signal may appear. A socket may be used, but it should be of a type having very short lead lengths, and in-the-board pins are definitely preferred. Proper bypassing is also essential. A total of at least $1\mu F$ of capacitance from V_{CC} to ground should be used on the board. Part of this $1\mu F$ may come from other bypasses installed to serve other circuits on the same board. In addition to the $1\mu F$ total, a bypass capacitor of $0.01\mu F$ should be connected directly from Pin 8 to Pin 5 of each 5082-4360 used on the board. These individual bypass capacitors must be low inductance disc ceramic. It is also important to have adequate bypassing for those circuits whose response is related to the signals produced in regenerative phase (positive feedback) with variations in the V_{CC} line voltage. If the common practice of having $1\mu F$ for each two circuits is adopted, there should be no problem, and much less bypassing will ordinarily suffice.

Common Mode Decoupling

Common mode decoupling can be significantly enhanced by running a ground trace midway between the rows of isolator terminals. This trace is, of course, connected to the output ground (Pin 5) of either the 5082-4350 or -4360. Its purpose is to cause electric potential at the input side to be coupled to ground at the output, rather than to some signal amplifying terminal. If no socket or if in-the-board socket pins are used, this ground lead may be simply a printed trace, but if a socket is used, the ground trace should be paralleled by a piece of grounded wire running up over the socket. When the common mode voltage is very high (>1000 V) the ground wire should be insulated to prevent electric discharge from the ground wire to the input terminals.

ANALOG APPLICATIONS

The fundamental requirement for an isolator to be used in analog circuits is that the output be a continuous monotonic function of the input signal. In the small signal transfer characteristics of Figure 10, the 5082-4350 isolator is shown to have this property, and the dynamic range extends from below 5 mA to the maximum allowable input currents.

Another requirement for some analog applications is that the device be linear. If inverse feedback is used, a considerable amount of device nonlinearity can be tolerated, but with an isolator, the purpose is to isolate the output from the input, so inverse feedback cannot be directly applied. It is therefore necessary to select the operating conditions carefully in order to avoid distortion.

Harmonic distortion is proportional to the change in gain through the excitation cycle and, therefore, the quiescent input current should be high enough that the gain does not change appreciably from what it is at the positive peak of the excitation cycle to what it is at the negative peak. By entering positive and negative peak values of the desired input current in the abscissa of Figure 10, the appropriate quiescent current may be selected for a given level of distortion tolerance.

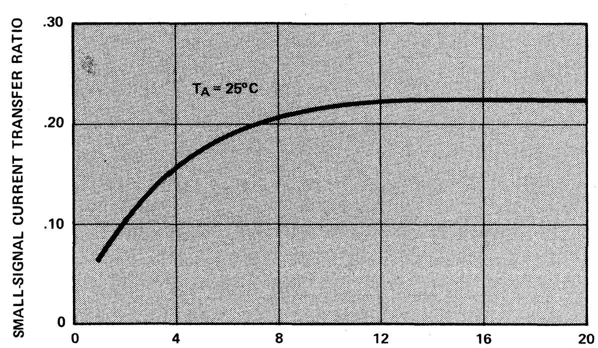


Figure 10. Typical Small-Signal Current Transfer Ratio

A suitable circuit for analog transmission of ac signals is shown in Figure 11. Here the base current of the transistor is adjusted to obtain the desired level of quiescent current. The value of the load resistor for the collector of the isolator's output transistor must be small enough so at the selected value of input quiescent current, the collector voltage will be high enough to accommodate the maximum excursion of the input current. The ac frequency response of the 5082-4350 in this circuit is given in the data sheet for various load resistors.

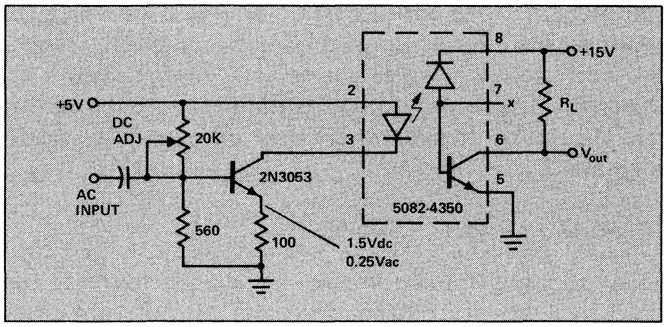


Figure 11. Optically Coupled AC Amplifier

Analog transmission of dc signals is also possible, but it requires the use of both positive and negative power supplies for both input and output to have zero offset. To minimize thermal drift of the offset, a differential pair of isolators is recommended; this has also a higher common mode rejection capability than the single-ended operation.

An example of such a system is shown in Figure 12, where the input signal can be non-inverting, inverting or differential. For the resistor values shown, the gain is unity, and the undistorted amplitude capability is one volt peak-to-peak, at a bandwidth of approximately 2MHz. The dc current through the input diode is approximately 1 mA and the 1N4001 diodes are used only for temperature compensation. This circuit is also capable of much

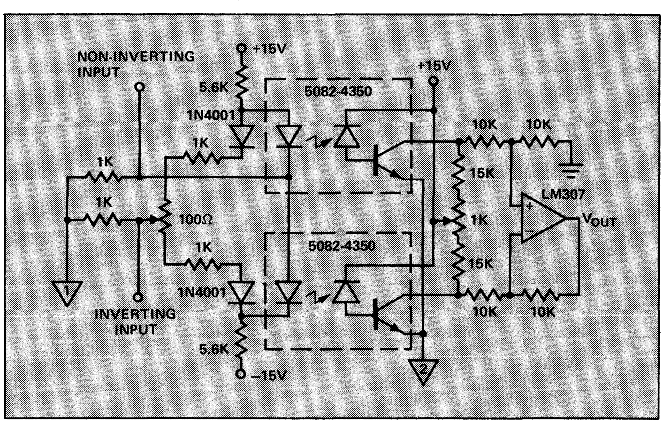


Figure 12. Optically Coupled DC Amplifier

higher gain than unity by operating the input at a somewhat higher quiescent current, but with the sacrifice of bandwidth, due to slew rate limitation in the operational amplifier.

TYPICAL APPLICATIONS

Ground loops involving peripheral equipment are effectively prevented by the use of optically coupled isolators. A typical situation is shown in Figure 13, in which the information on a set of BCD lines is made available at the electrically isolated outputs of the optically coupled isolators.

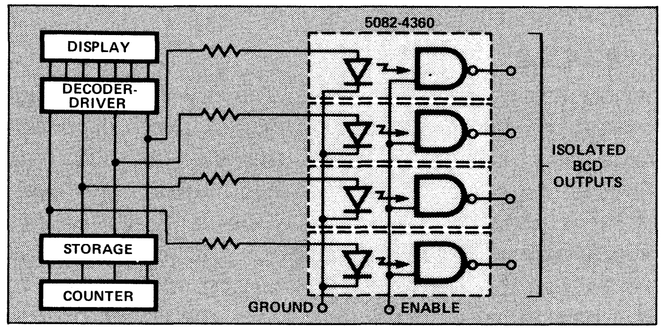
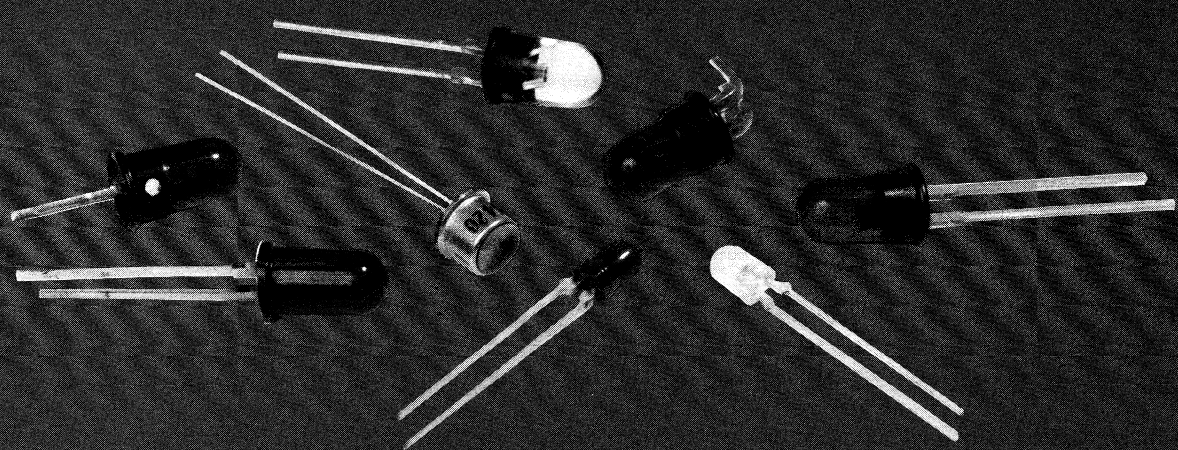


Figure 13. Strobed Optically Coupled Isolators

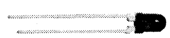
As long as the enable input remains high, the outputs will respond to changes of state at the inputs with logic delays which are typically 45ns, but which may vary from 30ns to as much as 75ns. This potential spread of logic delays, along with the potential anomalous words due to change-of-state glitching, make strobing an attractive technique. The 30 to 75ns delays in the isolators are due mainly to delays in generating and detecting the optical signals, and have no effect on the 15 to 25ns delays in response to changes at the enable inputs. Thus, without strobing of the enable inputs, the spread of logic transitions at the outputs may be as much as 45 ns due to the isolators plus whatever spread exists on the isolated input lines; with strobing the spread is reduced to 10ns, with a strobe **rate** limited only by the 75ns maximum delay in the isolator plus any spread present at the isolated inputs.

Although the use of the enable feature of the 5082-4360 is not always required, strobing of the enable inputs helps to eliminate the change-of-state glitches that are sometimes present on BCD and other word lines. When the enable inputs are held at logic '0' (low) the outputs will all be at logic '1' (high). When the enable inputs are high, the outputs will be low on only those isolators whose **isolated** input is at the logic '1' state; the other outputs will remain high.

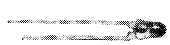
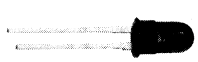
LED Lamps



Commercial LED Lamps

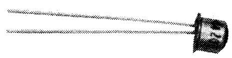
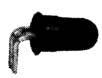
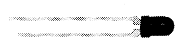
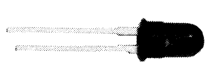
Device		Description	Package	Typical Luminous Intensity @ 20mA	Typical Forward Voltage @ 20mA	Page No.
	5082-4484	Red Diffused Lens PC Board Mountable	Plastic; 1/8" Dia. (T-1), Long Leads, .020" Sq.	0.8 mcd	1.6 Volts	37
	5082-4850	Red Diffused Lens Front Panel Mountable[1] Wire Wrappable Leads	Plastic; 1/5" Dia. (T-1-3/4), Long Leads,.025" Sq.			

Resistor LED Lamps

Device		Description	Package	Typical Luminous Intensity @ 20mA	Typical Forward Current @ 5V	Page No.
	5082-4468	Clear Diffused Lens PC Board Mountable	Plastic; 1/8" Dia. (T-1), Long Leads, .020" Sq.	0.8 mcd	16	39
	5082-4860	Red Diffused Lens Front Panel Mountable[1] Wire Wrappable Leads	Plastic; 1/5" Dia. (T-1-3/4), Long Leads,.025" Sq.			

NOTE 1: For clip mounting information, see page 43.

LED Lamps

Device		Description	Package	Typical Luminous Intensity @ 20 mA	Typical Forward Voltage @ 20 mA	Page No.
 5082-4420	5082-4420	Red Diffused Lens PC Board Mountable (1N5765)	Hermetic/TO-46, Aerospace and High Reliability Applications	0.7 mcd	1.6 Volts	34
 5082-4403/4440	5082-4440	Red Diffused Lens Front Panel Mountable [1]	Plastic; 1/5" Dia. (T-1-3/4), Short Leads,.030" Sq.			32
	5082-4444	Red Diffused Lens PC Board Mountable	Plastic; 1/5" Dia. (T-1-3/4), Bent Leads,.030" Sq.			
 5082-4415/4444	5082-4403	Red Diffused Lens Front Panel Mountable [1]	Plastic; 1/5" Dia. (T-1-3/4), Short Leads,.030" Sq.	1.2 mcd		
	5082-4415	Red Diffused Lens PC Board Mountable	Plastic; 1/5" Dia. (T-1-3/4), Bent Leads,.030" Sq.			
 5082-4480 Series	5082-4480	Red Diffused Lens PC Board Mountable	Plastic; 1/8" Dia. (T-1), Long Leads, .020" Sq.	0.8 mcd		35
	5082-4483	Clear Diffused Lens PC Board Mountable				
	5082-4486	Clear Lens PC Board Mountable				
 5082-4880 Series	5082-4880	Red Diffused Lens Front Panel Mountable [1]	Plastic; 1/5" Dia. (T-1-3/4), Long Leads,.025" Sq., Wire Wrappable Leads			41
	5082-4883	Clear Lens Front Panel Mountable [1]				
	5082-4886	Clear Diffused Lens Front Panel Mountable [1]				
	5082-4881	Red Diffused Lens Front Panel Mountable [1]		1.3 mcd		
	5082-4884	Clear Lens Front Panel Mountable [1]				
	5082-4887	Clear Diffused Lens Front Panel Mountable [1]				
	5082-4882	Red Diffused Lens Front Panel Mountable [1]		1.8 mcd		
	5082-4885	Clear Lens Front Panel Mountable [1]				
	5082-4888	Clear Diffused Lens Front Panel Mountable [1]				

NOTE 1. For clip mounting information, see page 43.

HEWLETT hp PACKARD

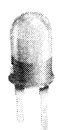
COMPONENTS

SOLID STATE LAMPS

5082-4403
5082-4440
INCLUDES -4415, -4444

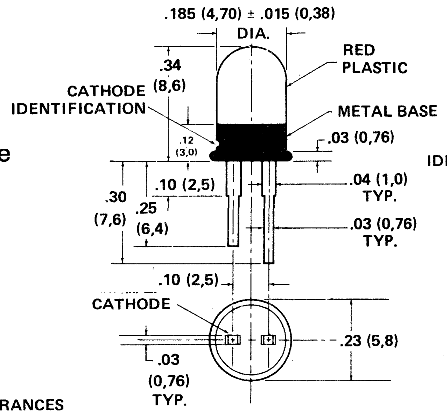
FEATURES

- Easily Panel Mountable
- High Brightness Over a Wide Viewing Angle
- Rugged Construction for Ease of Handling
- Sturdy Leads on 0.10-inch Centers
- IC Compatible/Low Power Consumption
- Long Life

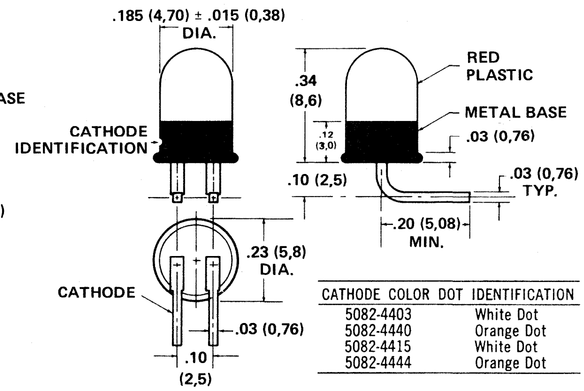


ACTUAL SIZE

TOLERANCES
xxx ± .005
xx ± .02



FOR PANEL MOUNTING
5082-4403
5082-4440



CATHODE COLOR DOT IDENTIFICATION	
5082-4403	White Dot
5082-4440	Orange Dot
5082-4415	White Dot
5082-4444	Orange Dot

FOR RIGHT ANGLE
PC BOARD MOUNTING
5082-4415
5082-4444

DESCRIPTION

The **5082-4403, -4415, -4440 and -4444** are plastic encapsulated Gallium Arsenide Phosphide Light Emitting Diodes. They radiate light in the 655 nanometer (red light) region.

The **5082-4403 and -4415** are LEDs with a red diffused plastic lens, providing high visibility for circuit board or panel mounting with a clip.

Both LEDs are designed for low power consumption, thus applicable for use in mobile and portable equipment.

The **5082-4440 and -4444** are economically priced LEDs with a red diffused plastic lens, providing a wide viewing angle for circuit board or panel mounting with clip. Both LEDs are designed for circuit status and other light indicating functions.

The **5082-4415 and -4444** have the added feature of a 90° lead bend for edge mounting on circuit boards.

MAXIMUM RATINGS (25°C)

DC Power Dissipation .... 100 mW
(Derate linearly from 50°C at 1.6mW/°C.)

DC Forward Current .... 50 mA

Peak Forward Current .... 1 Amp
(1 μsec pulse width, 300 pps)

Isolation Voltage (between lead and base) .... 300 V

Operating and Storage
Temperature Range .... −55°C to +100°C

Lead Soldering Temperature .... 230°C for 7 sec

ELECTRICAL CHARACTERISTICS (25°C)

Symbol	Parameters	5082-4403 5082-4415			5082-4440 5082-4444			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.		
I	Luminous Intensity	0.8	1.2		0.3	0.7		mcd	$I_F = 20$ mA
λ_{pk}	Wavelength	640	655	670	640	655	670	nm	Measurement at Peak
τ_s	Speed of Response		15			15		ns	
C	Capacitance		200			200		pF	$V_F = 0$, f = 1MHz
θ_{JC}	Thermal Resistance		270			270		°C/W	Junction to Cathode Lead
V_F	Forward Voltage		1.6	2.0		1.6	2.0	V	$I_F = 20$ mA
BV_R	Reverse Breakdown Voltage	3	10		3	10		V	$I_R = 10\ \mu A$

Mounting Instructions

The 5082-4707 is a black plastic mounting clip and retaining ring. It is designed to panel mount Hewlett Packard Solid State Lamps. This clip and ring combination is intended for installation in instrument panels up to .125" thick. For panels greater than .125", counterboring is required to the .125" thickness. Panel hole size is .250" (6,35) dia. The 5082-4707 replaces both the 5082-4409 and 5082-4418 mounting clips.

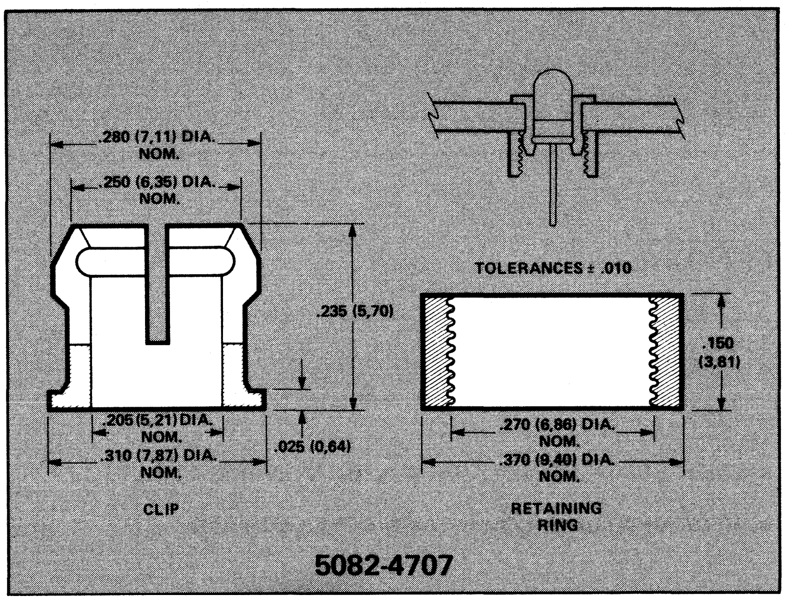


Figure 1.

PC Board Mounting Information

The 5082-4403 and 5082-4440 are intended to be versatile in their mounting capability, as shown in the sketches following. Various printed circuit board mounting means are shown in Figures 2, 3, and 4. The enlarged lead section provides a controlled spacing for perpendicular mounting shown in Figure 2.

For right angle mounting as shown in Figure 4, order either a 5082-4415 or 5082-4444. The leads are bent at 90°, ready for insertion.

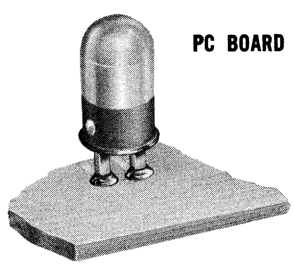


Figure 2. 5082-4403, -4440

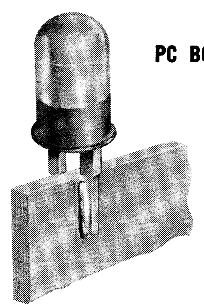


Figure 3. 5082-4403, -4440

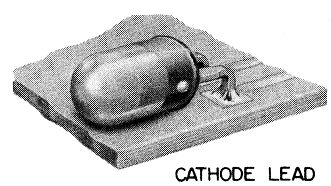
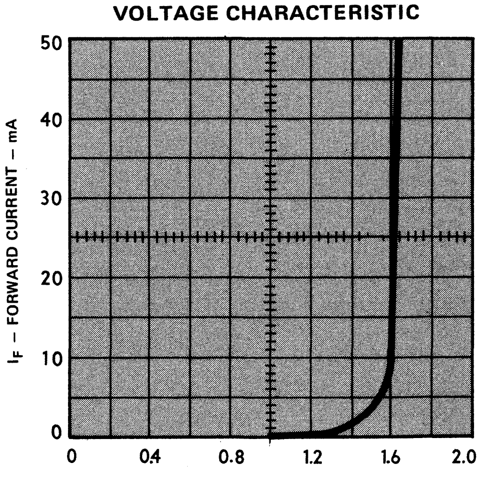
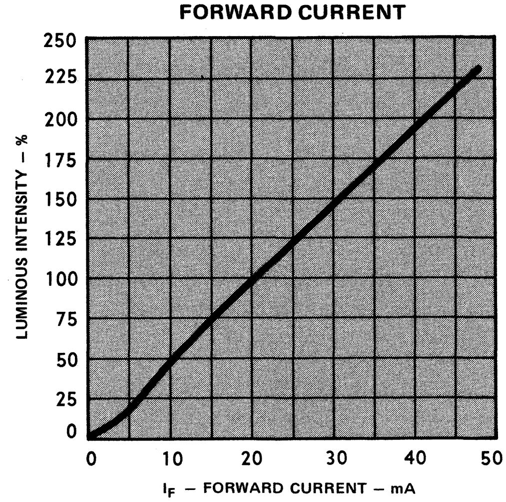


Figure 4. 5082-4415, -4444

FORWARD CURRENT – VOLTAGE CHARACTERISTIC



BRIGHTNESS VS. FORWARD CURRENT



HEWLETT hp PACKARD

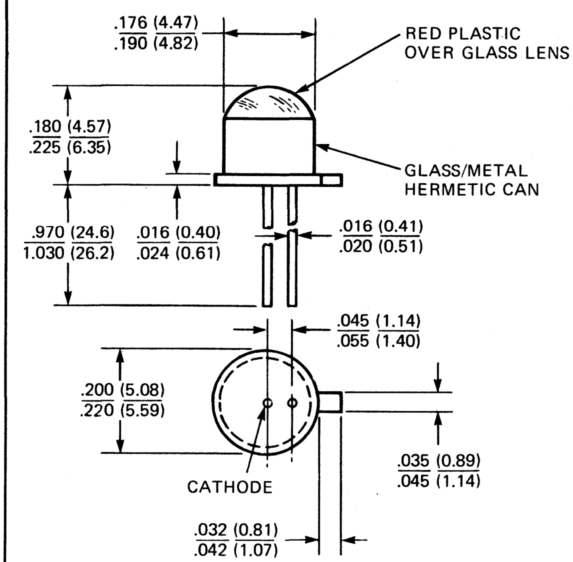
COMPONENTS

LIGHT EMITTING DIODE FOR HIGH-RELIABILITY APPLICATIONS

5082-4420

FEATURES

- DESIGNED FOR HIGH-RELIABILITY ENVIRONMENTS
- HERMETICALLY SEALED
- LONG LIFE
- HIGH BRIGHTNESS OVER A WIDE VIEWING ANGLE
- IC COMPATIBLE/LOW POWER CONSUMPTION



DESCRIPTION

5082-4420 — High performance Light Emitting Diode designed for high-reliability applications.

MAXIMUM RATINGS (25°C)

DC Power Dissipation . . . . 85 mW

DC Forward Current . . . . 50 mA

Peak Forward Current . . . . 1 Amp
(1 μsec pulse width, 300 pps)

Isolation Voltage (between lead and case) . . . . 500 V

Operating and Storage
Temperature Range . . . . −55°C to +100°C

Lead Soldering Temperature . . . . 230°C for 7 sec

ELECTRICAL CHARACTERISTICS (25°C)

Symbol	Parameters	5082-4420			Units	Test Conditions
		Min.	Typ.	Max.		
I	Luminous Intensity	500		3000	μcd	I_F = 20 mA
λ_{pk}	Wavelength		655		nm	Measurement at Peak
τ_s	Speed of Response		10		ns	
c	Capacitance		200	300	pF	V = 0 f = 1MHz
V_F	Forward Voltage		1.6	2.0	V	I_F = 20 mA
BV_R	Reverse Breakdown Voltage	4	5		V	I_R = 10 μA

HEWLETT PACKARD

COMPONENTS

SOLID STATE LAMPS (Mini-LED)

5082-4480 SERIES

Features

- HIGH INTENSITY – 0.8mcd TYPICAL
- WIDE VIEWING ANGLE
- SMALL SIZE T-1 DIAMETER (0.125")
- IC COMPATIBLE
- RELIABLE AND RUGGED

Description

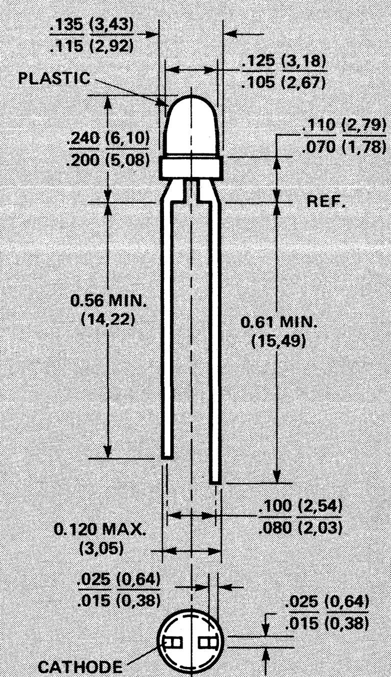
The 5082-4480 is a series of Gallium Arsenide Phosphide Light Emitting Diodes designed for applications where space is at a premium, such as in high density arrays.

The 5082-4480 series is available in three lens configurations.

5082-4480 – Red Diffused lens provides excellent on-off contrast ratio, high axial luminous intensity, and wide viewing angle.

5082-4483 – Same as 5082-4480, but Clear Diffused to mask red color in the "off" condition.

5082-4486 – Clear plastic lens provides a point source. Useful when illuminating external lens, annunciators, or photo-detectors.



PART NO.	LENS CONFIGURATION
5082-4480	Red Diffused
5082-4483	Clear Diffused
5082-4486	Clear Plastic

Maximum Ratings at $T_A = 25°C$

DC Power Dissipation 100mW
(Derate linearly from 50°C at 1.6mW/°C)

DC Forward Current 50mA

Peak Forward Current .... 1 Amp
(1 μsec pulse width, 300 pps)

Operating and Storage
Temperature Range .... –55°C to +100°C

Lead Soldering Temperature .... 230°C for 7 sec.

Electrical Characteristics at $T_A = 25°C$

Symbol	Parameters	5082-4480 5082-4483 5082-4486			Units	Test Conditions
		Min.	Typ.	Max.		
I	Luminous Intensity	0.3	0.8		mcd	$I_F = 20mA$
λ_{pk}	Wavelength		655		nm	Measurement at Peak
τ_s	Speed of Response		15		ns	
C	Capacitance		200		pF	$V_F = 0$, f = 1MHz
θ_{JC}	Thermal Resistance		270		°C/W	Junction to Cathode Lead
V_F	Forward Voltage		1.6	2.0	V	$I_F = 20mA$
BV_R	Reverse Breakdown Voltage	3	10		V	$I_R = 10\mu A$

Mounting Information

The 5082-4480 series is designed for flush PC board mounting. It is ideally suited for large area arrays.

The -4480 is mounted in 0.045" holes on either 0.090" or 0.100" centers.

The -4480 is easily laid out in large area X-Y addressable arrays, with the lamps on 0.125" (minimum) centers. Figure 1 illustrates a typical PC board layout for such an array. Note that it is preferable to mount the lamps with their leads aligned on the diagonal. Typical mounting dimensions are included in the sketch.

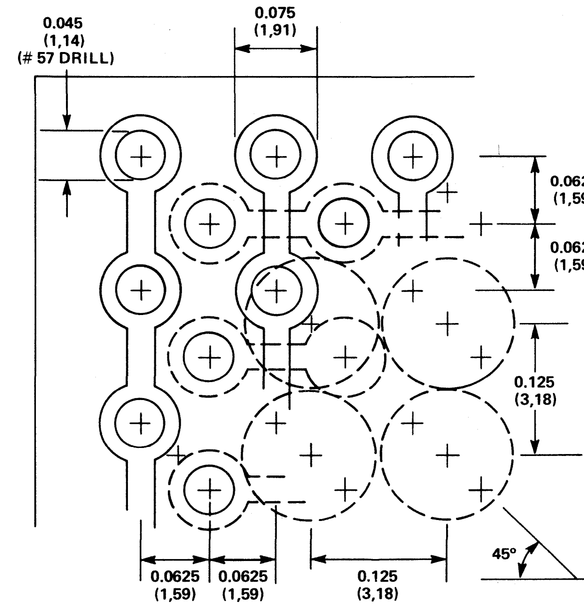
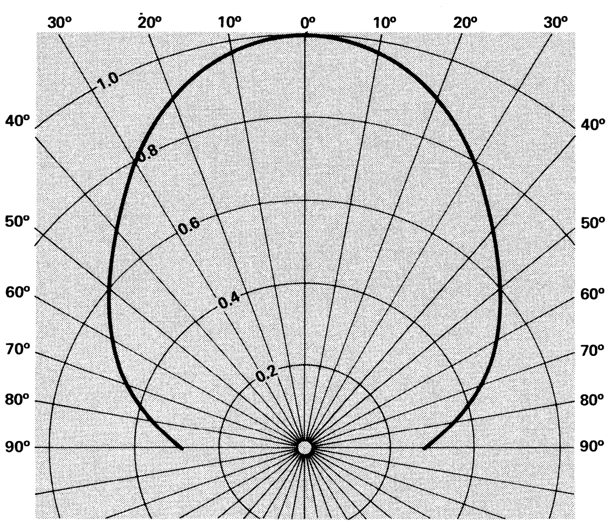
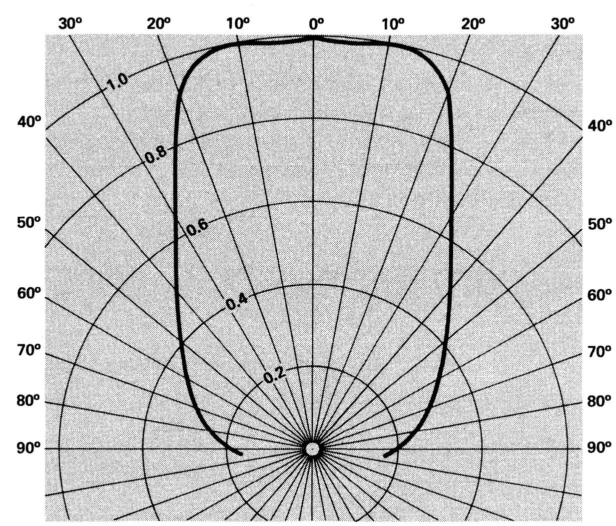


Figure 1. Typical PC board layout for an X-Y addressable array. LED's may be spaced as closely as 0.125" on centers.

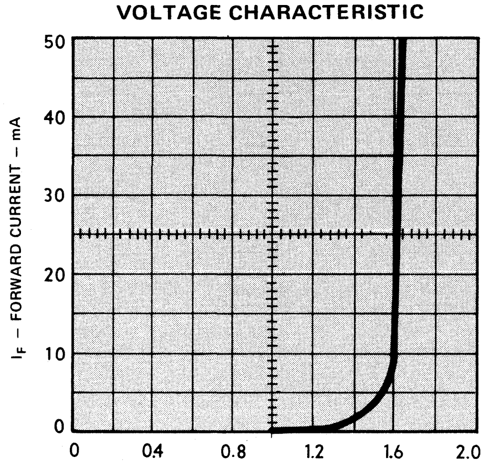
RELATIVE LUMINOUS INTENSITY VERSUS ANGULAR DISPLACEMENT 5082-4480 AND 5082-4483



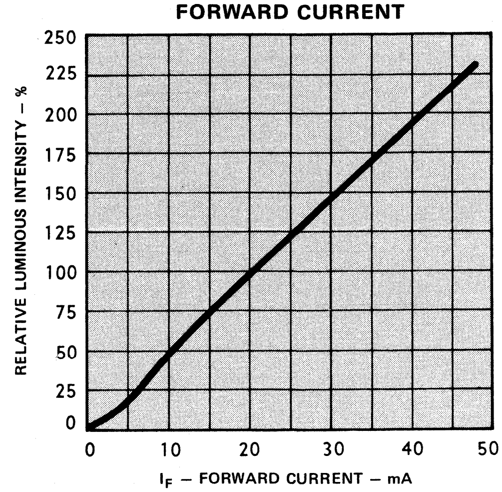
RELATIVE LUMINOUS INTENSITY VERSUS ANGULAR DISPLACEMENT 5082-4486



FORWARD CURRENT – VOLTAGE CHARACTERISTIC



LUMINOUS INTENSITY VS. FORWARD CURRENT

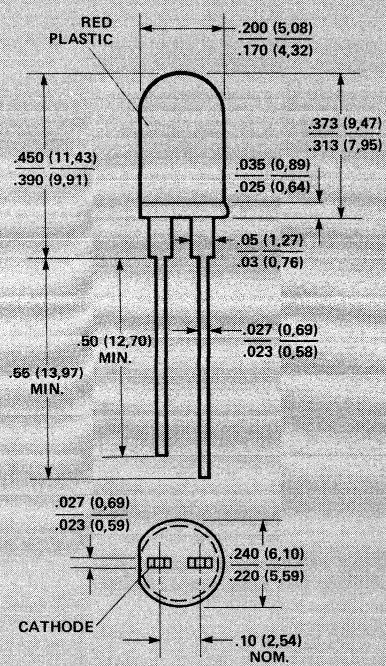


HEWLETT PACKARD

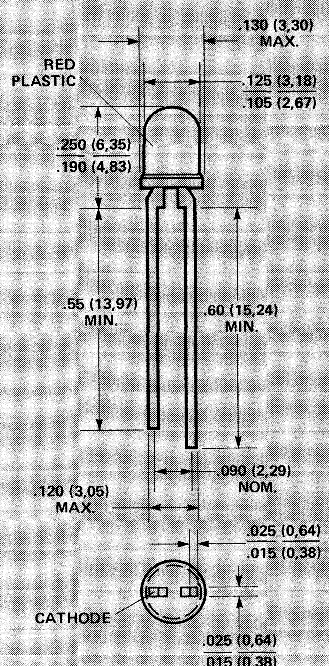
COMPONENTS

COMMERCIAL LIGHT EMITTING DIODES

5082-4850 5082-4484



5082-4850



5082-4484

Features

- LOW COST – BROAD APPLICATION
- LONG LIFE – SOLID STATE RELIABILITY
- LOW POWER REQUIREMENTS – 20mA @ 1.6V
- HIGH LIGHT OUTPUT – 0.8mcd TYPICAL

Description

The 5082-4850 and 5082-4484 are Gallium Arsenide Phosphide Light Emitting Diodes intended for **High Volume/Low Cost** applications such as indicators for appliances, automobile instrument panels and many other commercial uses.

The 5082-4850 fits the T-1¾ lamp size, has a red diffused lens and can be panel mounted.

The 5082-4484 fits the T-1 lamp size, has a red diffused lens and is ideal where space is at a premium, such as high density arrays.

Maximum Ratings at T_A=25°C

DC Power Dissipation 100mW
(Derate linearly from 50°C at 1.6mW/°C)

DC Forward Current 50mA

Peak Forward Current 1Amp
(1μsec pulse width, 300pps)

Operating and Storage
Temperature Range .... –55°C to +100°C

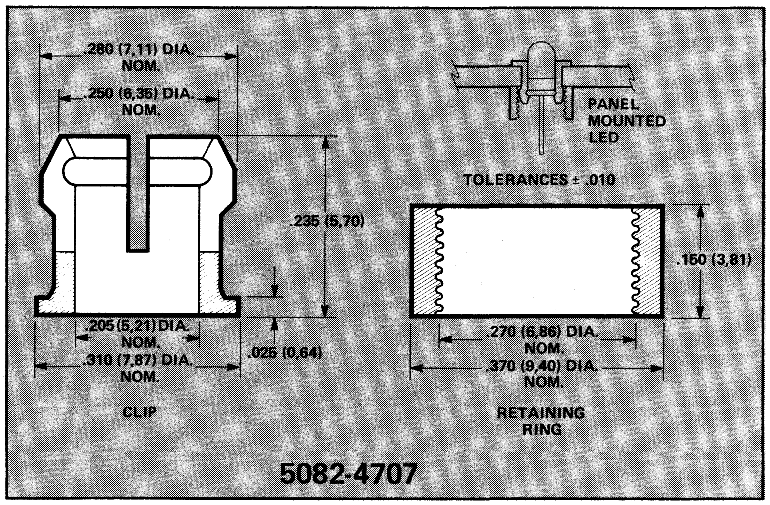
Lead Soldering Temperature .... 230°C for 7 sec.

Electrical Characteristics at T_A=25°C

Symbol	Parameters	5082-4850 Min.	5082-4850 Typ.	5082-4850 Max.	5082-4484 Min.	5082-4484 Typ.	5082-4484 Max.	Units	Test Conditions
I_v	Luminous Intensity		0.8			0.8		mcd	I_F = 20mA
λ_{pk}	Wavelength		655			655		nm	Measurement at Peak
τ_s	Speed of Response		10			10		ns	
C	Capacitance		100			100		pF	V_F = 0, f = 1MHz
V_F	Forward Voltage		1.6	2.0		1.6	2.0	V	I_F = 20mA
BV_R	Reverse Breakdown Voltage	3	10		3	10		V	I_R = 100μA

Mounting Instructions

The 5082-4707 is a black plastic mounting clip and retaining ring. It is designed to panel mount Hewlett Packard Solid State Lamps. This clip and ring combination is intended for installation in instrument panels up to .125" thick. For panels greater than .125", counterboring is required to the .125" thickness. Panel hole size is .250" (6,35) dia. The 5082-4707 replaces both the 5082-4409 and 5082-4418 mounting clips.



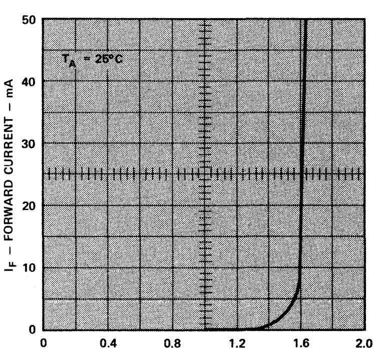


Figure 1. Typical Forward Current Versus Voltage Characteristic.

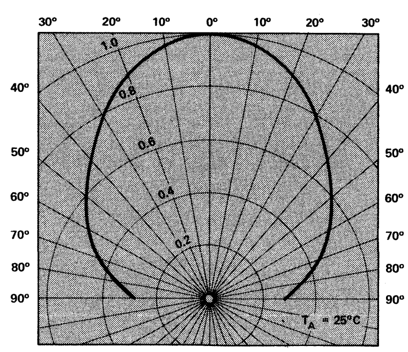


Figure 2. Typical Relative Luminous Intensity Versus Angular Displacement.

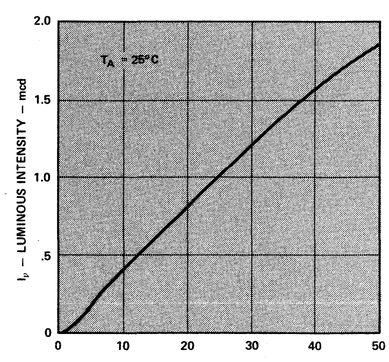
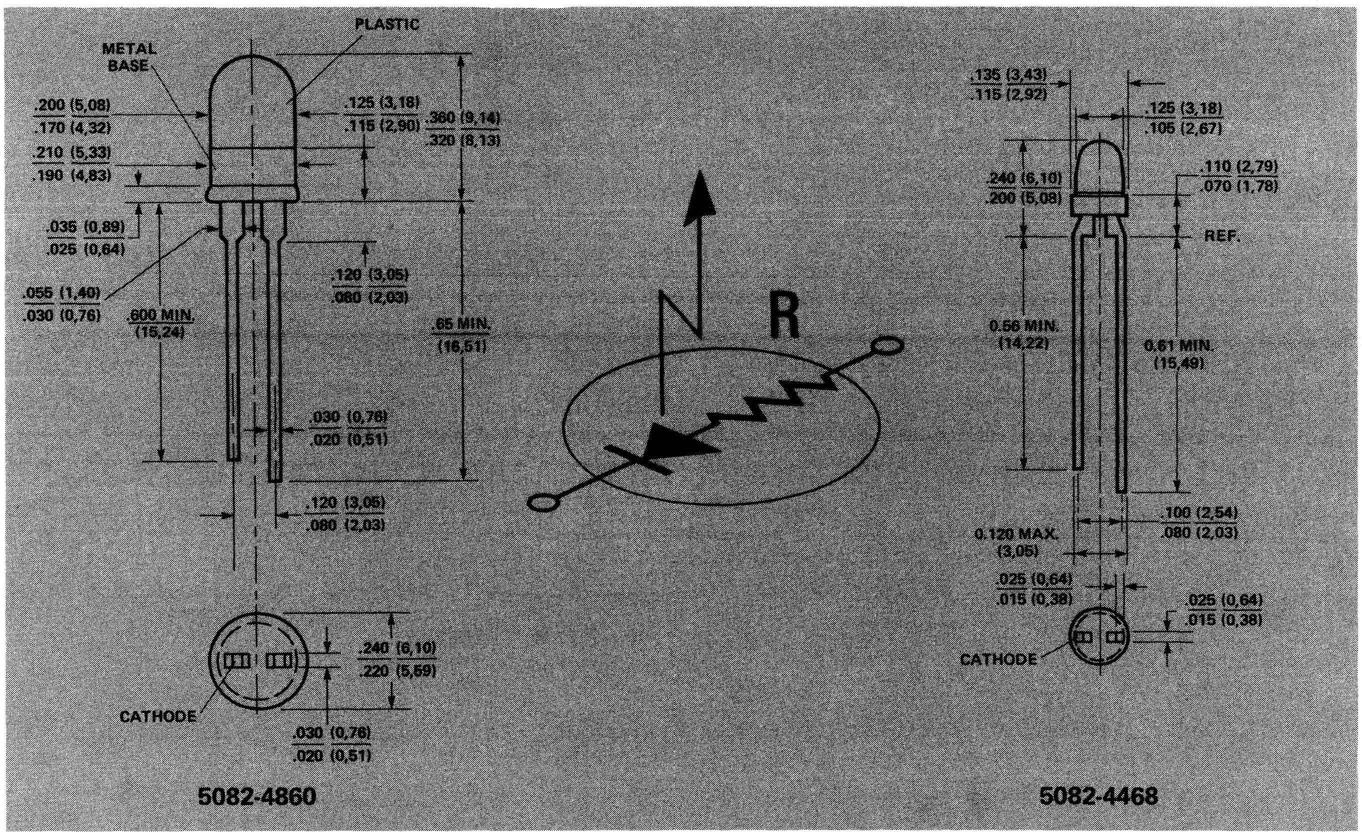


Figure 3. Typical Luminous Intensity Versus Forward Current

HEWLETT PACKARD

COMPONENTS

RESISTOR LEDs 5082-4860 5082-4468



Features

- TTL COMPATIBLE – 16mA @ 5 VOLTS TYPICAL
- INTEGRAL CURRENT LIMITING RESISTOR
- T-1 (.125") SIZE AND T-1¾ (.200") SIZE
- RUGGED AND RELIABLE

Description

The HP Resistor-LED series provides an integral current limiting resistor in series with the LED. Applications include panel mounted indicators, cartridge indicators, and lighted switches.

The 5082-4860 is a standard red diffused .200" diameter (T-1¾ size) LED, with long wire wrappable leads.

The 5082-4468 is a clear diffused .125" diameter (T-1 size) LED.

Maximum Ratings (T_A = 25°C unless otherwise stated)

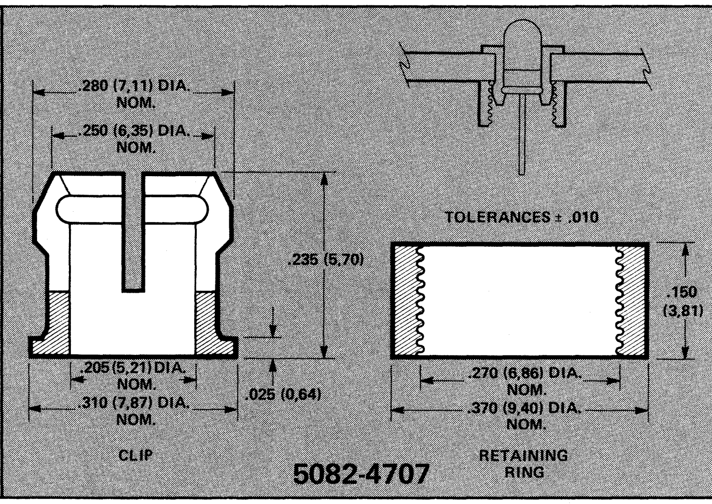
DC Forward Voltage [Derate linearly to 5V @ 100°C]	7.5V
Reverse Voltage	7V
Isolation Voltage [between lead and base of the 5082-4860]	300V
Operating and Storage Temperature Range	–55°C to +100°C
Lead Soldering Temperature	230°C for 7 sec.

Electrical Characteristics at $T_A = 25°C$

Symbol	Parameters	5082-4860/-4468 Min.	Typ.	Max.	Units	Test Conditions
I_v	Luminous Intensity	0.3	0.8		mcd	$V_F = 5.0V$
λ_{pk}	Wavelength		655		nm	Measurement at Peak
τ_s	Speed of Response		15		ns	
I_F	Forward Current		16	20	mA	$V_F = 5.0V$
BV_R	Reverse Breakdown Voltage	3			V	$I_R = 10\mu A$

Mounting Instructions

The 5082-4707 is a black plastic mounting clip and retaining ring. It is designed to panel mount Hewlett Packard Solid State Lamps. This clip and ring combination is intended for installation in instrument panels up to .125″ thick. For panels greater than .125″, counterboring is required to the .125″ thickness. Panel hole size is .250″ (6,35) dia. The 5082-4707 replaces both the 5082-4409 and 5082-4418 mounting clips.



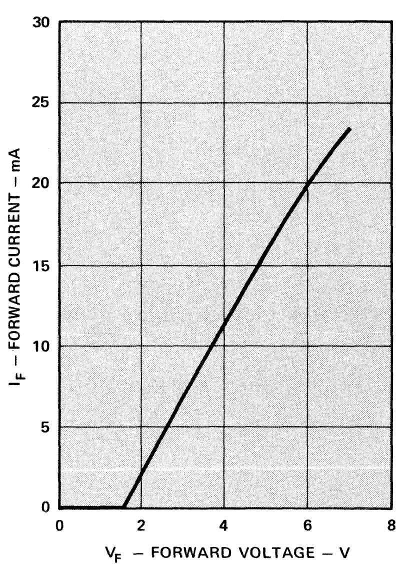


Figure 1. Typical DC Forward Current – Voltage Characteristic

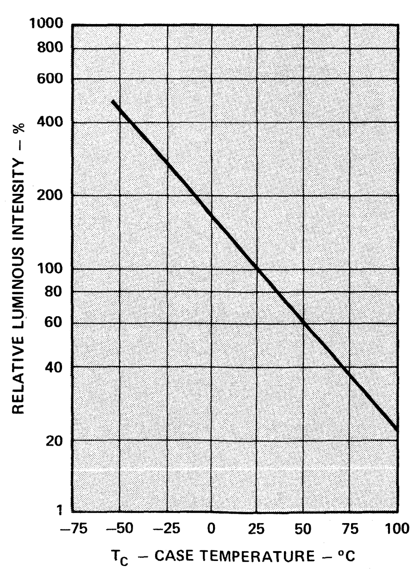


Figure 2. Relative Luminosity vs. Case Temperature

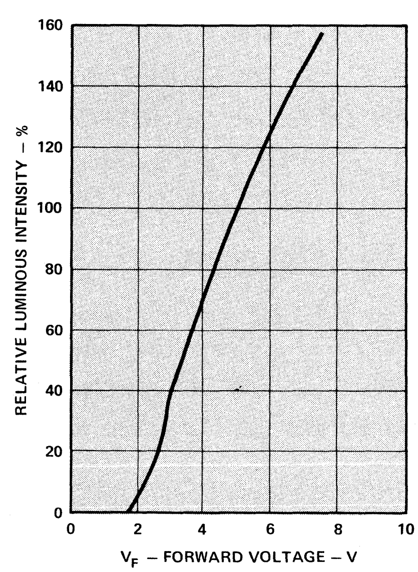


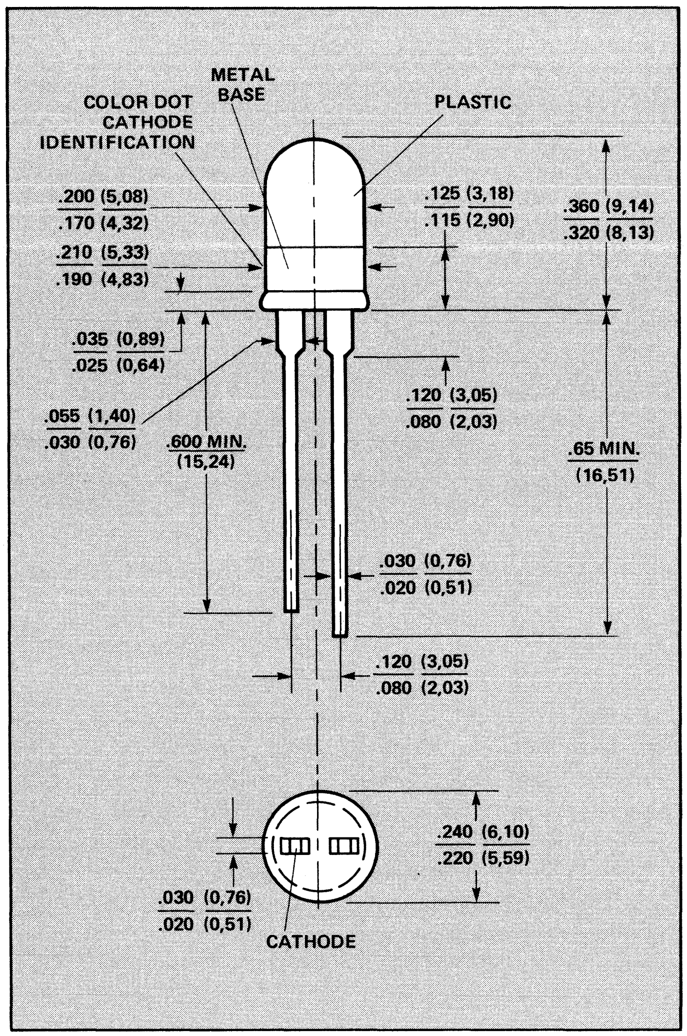
Figure 3. Relative Luminous Intensity vs. Voltage

HEWLETT hp PACKARD
COMPONENTS

SOLID STATE LAMPS — 5082-4880 SERIES

FEATURES

- WIRE WRAPPABLE
- EASILY PANEL MOUNTABLE; CLIP AVAILABLE
- STURDY WELDABLE LEADS -- ON 0.10 INCH CENTERS
- HIGH BRIGHTNESS OVER A WIDE VIEWING ANGLE
- RUGGED CONSTRUCTION FOR EASE OF HANDLING
- IC COMPATIBLE/LOW POWER CONSUMPTION
- LONG LIFE



DESCRIPTION

Wire Wrappable

The 5082-4880 series is designed to be wire wrapped with the Gardner Denver Models 14R2, 14XL1, and 14XA2 or equivalent. The LED can be panel or PC mounted and the leads directly wire wrapped without the use of a socket.

Light Output Selection

The 5082-4880 series is available with graded light output levels, so you can select the proper uniform light level for your application.

Lens Appearance

The 5082-4880 series is available in three different lens configurations. These are Red Diffused, Clear Diffused, and Clear.

The Red Diffused lens provides an excellent off/on contrast ratio. The Clear lens is designed for applications where a point source is desired. It is particularly useful where the light must be focused or diffused with external optics. The Clear Diffused lens is useful in masking the red color in the off condition.

LED SELECTION GUIDE

MINIMUM LIGHT OUTPUT (mcd)	LENS TYPE		
	Red Diffused Lens	Clear Plastic Lens	Clear Diffused Lens
0.5	5082-4880	5082-4883	5082-4886
1.0	5082-4881	5082-4884	5082-4887
1.6	5082-4882	5082-4885	5082-4888

MAXIMUM RATING (25°C)

DC Power Dissipation . . . . .100 mW

DC Forward Current 50mA

Peak Forward Current . . . . 1 Amp
(1 μsec pulse width, 300 pps)

Isolation Voltage (between lead and case) . . . 300V

Operating and Storage
Temperature Range . . . . . . –55°C to +100°C

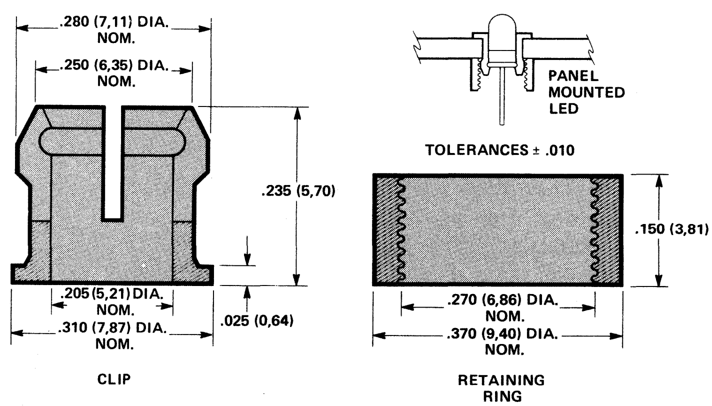
Lead Soldering Temperature . . . . 230°C for 7 sec

ELECTRICAL CHARACTERISTICS (25°C)

Symbol	Parameters	5082 - 4880 5082 - 4883 5082 - 4886			5082 - 4881 5082 - 4884 5082 - 4887			5082 - 4882 5082 - 4885 5082 - 4888			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_v	Luminous Intensity	0.5	0.8		1.0	1.3		1.6	1.8		mcd	I_F = 20 mA
I_v	Luminous Intensity								0.8		mcd	I_F = 10 mA
λ_{pk}	Wavelength		655			655			655		nm	Measurement at Peak
τ_s	Speed of Response		10			10			10		ns	
C	Capacitance		200			200			200		pF	
θ_{JC}	Thermal Resistance		270			270			270		$^oC/W$	Junction to Cathode Lead
V_F	Forward Voltage		1.6	2.0		1.6	2.0		1.6	2.0	V	I_F = 20 mA
BV_R	Reverse Breakdown Voltage	3	4		3	4		3	4		V	I_R = 10 μA

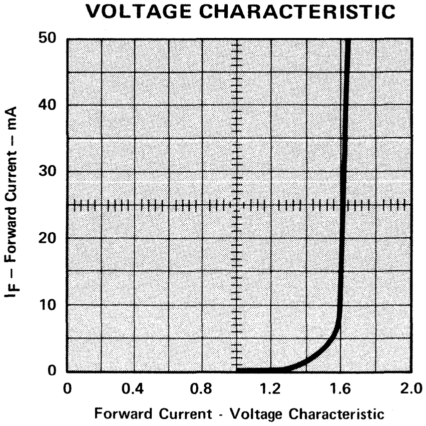
MOUNTING INFORMATION

The 5082-4707 is a black plastic mounting clip and retaining ring. It is designed to panel mount Hewlett Packard Solid State Lamps. This clip and ring combination is intended for installation in instrument panels up to .125" thick. For panels greater than .125", counterboring is required to the .125" thickness. Panel hole size is .250" (6,35) dia. The 5082-4707 replaces both the 5082-4409 and 5082-4418 mounting clips.

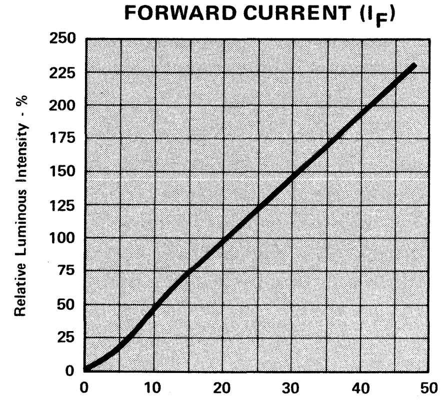


5082-4707

FORWARD CURRENT VERSUS VOLTAGE CHARACTERISTIC



LUMINOUS INTENSITY VERSUS FORWARD CURRENT (I_F)



HEWLETT hp PACKARD

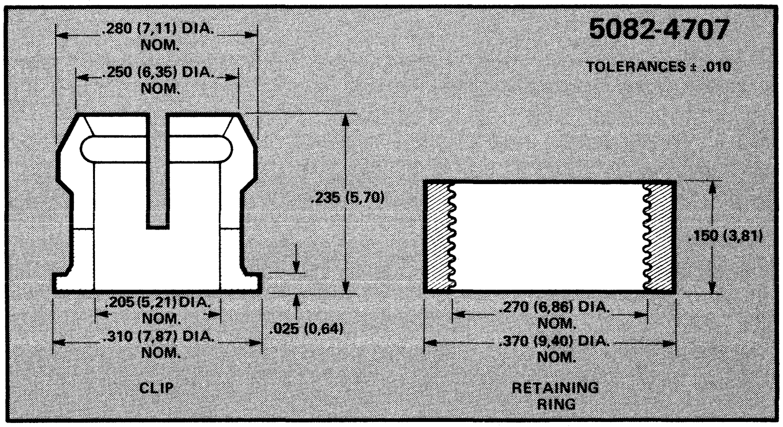
COMPONENTS

CLIP AND RETAINING RING FOR PANEL MOUNTED LEDs

5082-4707

Description

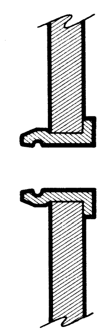
The 5082-4707 is a black plastic mounting clip and retaining ring. It is designed to panel mount Hewlett Packard Solid State Lamps. This clip and ring combination is intended for installation in instrument panels up to .125" thick. For panels greater than .125", counterboring is required to the .125" thickness. Panel hole size is .250" (6,35) dia. The 5082-4707 replaces both the 5082-4409 and 5082-4418 mounting clips.



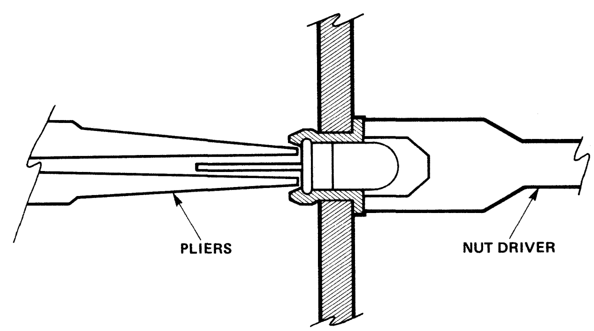
Mounting Instructions

1. Drill a .250" dia. hole in the panel. Deburr but do not chamfer the edges of the hole.

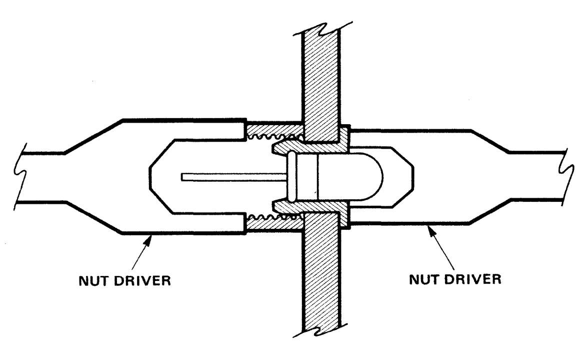
2. Press the panel clip into the hole from the front of the panel.



3. Press the LED into the clip from the back. Use blunt long nose pliers to push on the LED. Do not use force on the LED leads. A tool such as a nut driver may be used to press on the clip.[1]

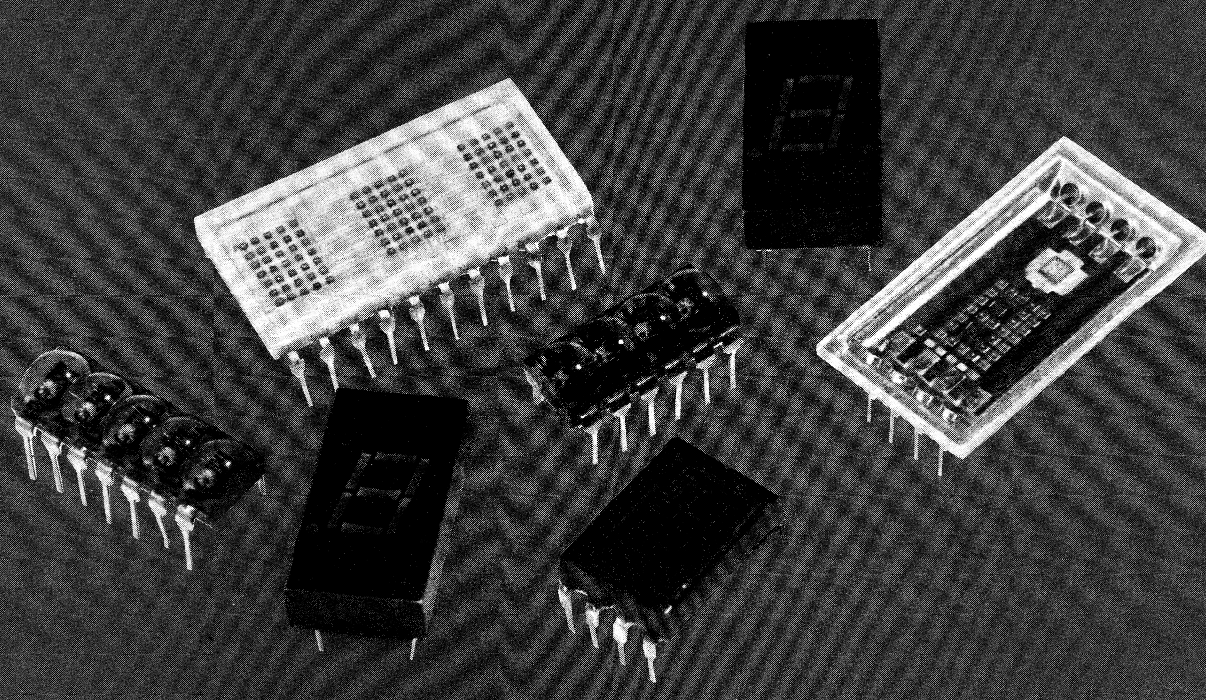


4. Slip a plastic retaining ring onto the back of the clip and press tight using tools such as two nut drivers.[1]

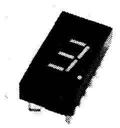
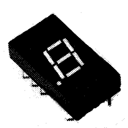
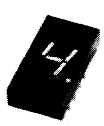
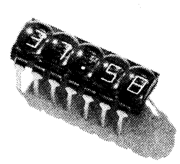
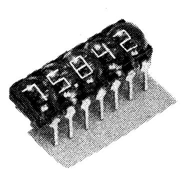


NOTE 1:
A nut driver is a hand tool that is a combination of a screwdriver handle and a socket wrench.

LED Displays

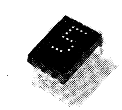
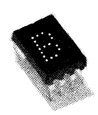
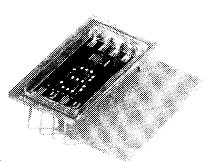
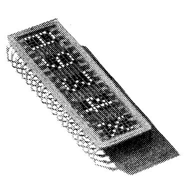
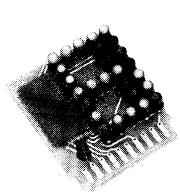


LED Displays

Device		Description	Package	Application	Page No.
 5082-7730	5082-7730	.3" Single Digit Numeric, Common Anode, LHDP	14 Pin Epoxy .3" DIP	■ General Purpose Market □ Test Equipment □ Digital Clocks □ Clock Radios □ TV Receivers □ Business Machines (For further information, see 5082-7730 Series Applications Brief, pg. 95.)	66
 5082-7731	5082-7731	.3" Single Digit Numeric, Common Anode, RHDP			
 5082-7740	5082-7740	.3" Single Digit Numeric, Common Cathode, RHDP	10 Pin Epoxy .3" DIP		69
 5082-7405	5082-7402	.11" 7 Segment Display 3 Digits Right,[1] Centered Decimal Point	12 Pin Epoxy .3" DIP	■ Small Display Market □ Portable/Battery Powered Instruments □ Portable Calculators (For further information, see Application Note 937, page 89.)	60
	5082-7403	.11" 7 Segment Display 3 Digits Left,[1] Centered Decimal Point			
	5082-7404	.11" 7 Segment Display 4 Digits, Centered Decimal Point			
	5082-7405	.11" 7 Segment Display 5 Digits, Centered Decimal Point	14 Pin Epoxy .3" DIP		
 5082-7415	5082-7412	.11" 7 Segment Display 3 Digit Right,[1] RHDP	12 Pin Epoxy .3" DIP		
	5082-7413	.11" 7 Segment Display 3 Digit Left,[1] RHDP			
	5082-7414	.11" 7 Segment Display 4 Digit, RHDP			
	5082-7415	.11" 7 Segment Display 5 Digit, RHDP	14 Pin Epoxy .3" DIP		

NOTE 1: Three Digit Displays are mounted in four-digit packages with digits placed to the left or right. (See page 62.)

LED Displays

Device		Description	Package	Application	Page No.
 5082-7300	5082-7300	.29″ 4 x 7 Single Digit Numeric, RHDP, Built-In Decoder/Driver/Memory	8 Pin Epoxy .6″ DIP	■ General Purpose Market □ Test Equipment □ Business Machines □ Medical □ Computer Peripherals □ Avionics (For further information, see Application Note 934 page 85)	56
	5082-7302	.29″ 4 x 7 Single Digit Numeric, LHDP, Built-In Decoder/Driver/Memory			
 5082-7340	5082-7304	.29″ Overrange Character Plus/Minus Sign			
	5082-7340	.29″ 4 x 7 Single Digit Hexadecimal, Built-In Decoder/Driver/Memory			
 5082-7000	5082-7000	.27″ 5 x 7 Single Digit Numeric, LHDP, Built-In Decoder/Driver	8 Pin Hermetic .100″ Pin Centers	■ General Military Applications ■ High Reliability Applications	48
	5082-7001	.27″ 5 x 7 Three Digit Numeric, LHDP, Built-In Decoder/Driver	24 Pin Hermetic .100″ Pin Centers		
	5082-7018	Single Indicator Plus/Minus Sign	8 Pin Hermetic .100″ Pin Centers		
 5082-7102	5082-7100	.29″ 5 x 7 Three Digit Alphanumeric	22 Pin Hermetic .6″ DIP	■ General Purpose Market □ Business Machines □ Calculators □ Solid State CRT ■ High Reliability Applications (For further information, see Application Note 931, page 71.)	52
	5082-7101	.29″ 5 x 7 Four Digit Alphanumeric	28 Pin Hermetic .6″ DIP		
	5082-7102	.29″ 5 x 7 Five Digit Alphanumeric	36 Pin Hermetic .6″ DIP		
 5082-7500	5082-7500	1.5″ 5 x 7 Single Digit LHDP, Built-In Decoder/Driver	PC Board 10 Pin Edge Card Connector (.156″ Centers)	■ General Purpose Market □ Test Equipment □ Medical Equipment ■ Industrial Controls	64

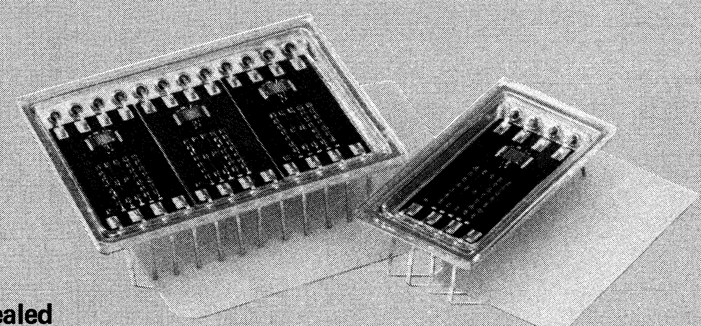
HEWLETT PACKARD
COMPONENTS

SOLID STATE LED NUMERIC INDICATOR

5082-7000

Features

- IC Compatible
- Includes Decoder/Driver
  - 8421 BCD Input
- 5 x 7 LED Matrix Character
  - Human Factors Engineered
- Variable Light Output
- Long Operating Life
- Small Size - 1.06 x 0.59 x 0.15 Inches
- Rugged, Shock Resistant, Hermetically Sealed
- Designed to Meet MIL Standards



Description

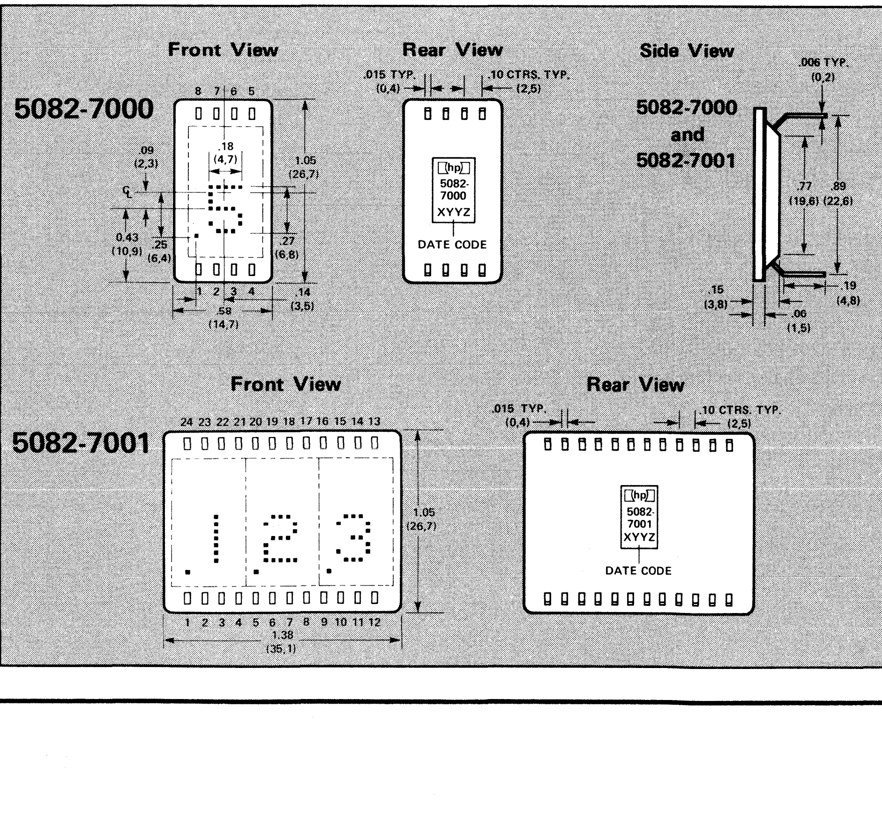
The HP 5082-7000 series solid state numeric indicators with built-in decoder/driver provides a hermetically sealed .27" display for use in military or adverse industrial environments. Typical applications include ground, airborne and shipboard equipment, fire control systems, and space flight digital displays.

The 5082-7000 is a single digit modified 5 x 7 LED matrix display with built-in decoder/driver that indicates the numerals 0-9 when presented with a BCD code. The BCD code is negative logic and blanks are displayed for all remaining invalid codes. A separate input is provided for variable luminous intensity control. An externally current limited left-hand decimal point is also provided.

The 5082-7001 is identical to the -7000, except that three digits are in a hermetic package.

The 5082-7018 is the companion plus/minus sign in a -7000 type hermetic package. Plus/minus indications require only that voltage be applied to two input pins. Luminous intensity is variable by changing the DC drive voltage.

Package Dimensions



FUNCTION	PIN 5082-7000	5082-7001 Digit 1	5082-7001 Digit 2	5082-7001 Digit 3
Input 1	1	1	5	9
Input 2	8	24	20	16
Input 4	5	21	17	13
Input 8	4	4	8	12
V_{CC}	7	23	19	15
V_{LED}	3	3	7	11
V_{DP} (Decimal Point)	2	2	6	10
Ground	6	22	18	14

NOTES:
1. Unless otherwise specified, the tolerance on all dimensions is ±.015 inches and (±0,38 mm.).
2. All dimensions in inches and (millimeters).

Absolute Maximum Ratings*

Description	Symbol	Min.	Max.	Unit
Storage Temperature, Ambient	T_S	−65	+100	°C
Operating Temperature, Case	T_C	−55	+95	°C
Logic Supply Voltage to Ground	V_{CC}	−0.5	+7.0	V
Logic Input Voltage	V_{in}	−0.5	5.5 [1]	V
LED Supply Voltage to Ground	V_{LED}	−0.5	+4.2	V
Decimal Point Current	I_{DP}		−10	mA

Note 1: V_{in} Potential not to exceed V_{CC} by more than 0.5V at any time.

Recommended Operating Conditions*

Description	Symbol	Min.	Nom.	Max.	Unit
Logic Supply Voltage	V_{CC}	4.75	5.0	5.25	V
LED Supply Voltage, Display Off	V_{LED}	−0.5	0	+1.0	V
LED Supply Voltage, Display On	V_{LED}	2.5	4.0	4.2	V
Decimal Point Current	I_{DP} [1]	0	−5.0	−10.0	mA
Logic Input Voltage, "H" State	$V_{in\,(H)}$	2.8		5.0	V
Logic Input Voltage, "L" State	$V_{in\,(L)}$	0		0.6	V

Note 1: Decimal point current must be externally current limited.

Electrical/Optical Characteristics*

(T_C = 0°C to 70°C, unless otherwise specified)

Description	Symbol	Test Condtions	Min.	Typ.	Max.	Unit
Logic Supply Current	I_{CC}	V_{CC} = 5.25V		50	75	mA
LED Supply Current	I_{LED}	V_{LED} = 4.2V V_{CC} = 5.25V		100 [1]	230	mA
LED Supply Current	I_{LED}	V_{LED} = 3.5V V_{CC} = 5.25V		70 [1]		mA
Logic Input Current, "H" State	$I_{in\,(H)}$	V_{CC} = 5.25V V_{in} = 2.8V		−300	−500	μA
Logic Input Current, "L" State	$I_{in\,(L)}$	V_{CC} = 5.25V V_{in} = 0.4V		−2	−4	mA
Decimal Point Voltage Drop	$V_{LED} - V_{DP}$	I_{DP} = −10mA		1.6	2.0	V
Power Dissipation	P_T	V_{CC} = 5.25V V_{LED} = 4.25V		0.7 [1]	1.4	W
Power Dissipation	P_T	V_{CC} = 5.25V, V_{LED} = 3.5V		0.5 [1]		W
Luminous Intensity per LED (Digit Average)	I_ν	V_{LED} = 4.2V [2]	40	100		μcd
Luminous Intensity per LED (Digit Average)	I_ν	V_{LED} = 3.5V [2]		50		μcd
Peak Wavelength	λ_{peak}	T_C = 25°C		655		nm
Spectral Halfwidth	$\Delta\lambda_{1/2}$	T_C = 25°C		30		nm
Weight				3.1		gram

Note 1. With average number of LED's lighted.
Note 2. T_C = 25°C.
*Values apply to the 5082-7000 or each digit of the 5082-7001.

Truth Table

Character	Logic X8	X4	X2	X1	
0	H	H	H	H	0
1	H	H	H	L	1
2	H	H	L	H	2
3	H	H	L	L	3
4	H	L	H	H	4
5	H	L	H	L	5
6	H	L	L	H	6
7	H	L	L	L	7
8	L	H	H	H	8
9	L	H	H	L	9
Blank	L	H	L	H	
Blank	L	H	L	L	
Blank	L	L	H	H	
Blank	L	L	H	L	
Blank	L	L	L	H	
Blank	L	L	L	L	

Note: L = 0 to 0.6V
H = 2.8 to 5.0V

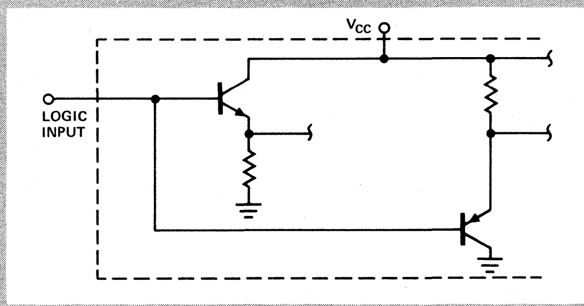


Figure 1. Equivalent circuit of 5082-7000 Decoder as seen from each logic input line.

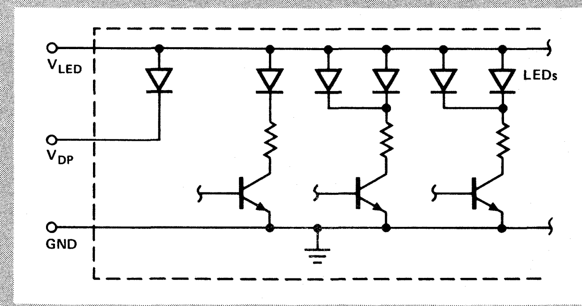


Figure 2. Equivalent circuit as seen from LED and decimal point drive lines.

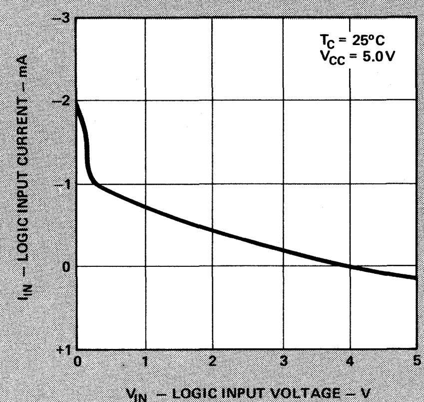


Figure 3. Typical BCD input current as a function of input voltage.

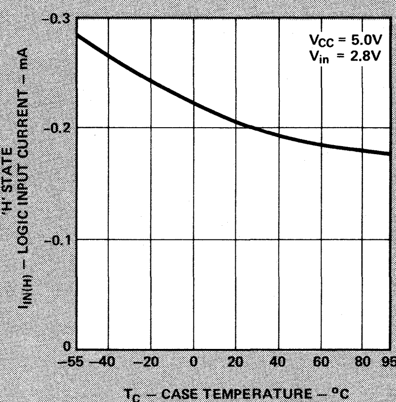


Figure 4. Typical logic "H" input current as a function of case temperature.

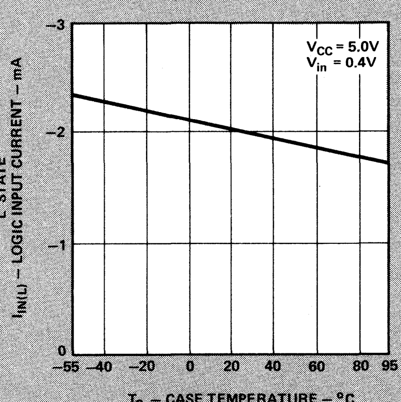


Figure 5. Typical logic "L" input current as a function of case temperature.

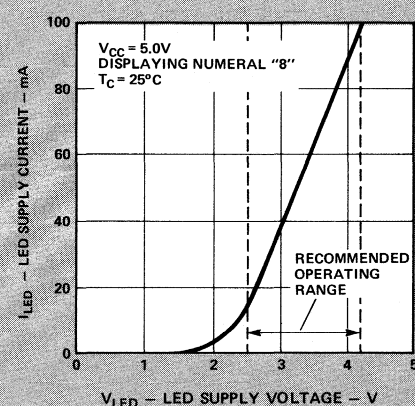


Figure 6. Typical I_{LED} as a function of V_{LED}.

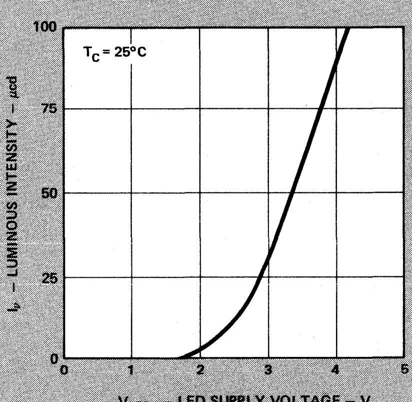


Figure 7. Typical Luminous Intensity per LED as a function of V_{LED} (Digit Average).

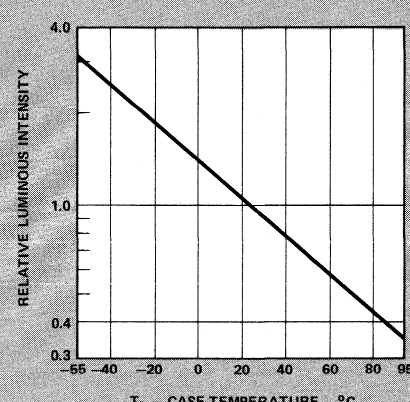


Figure 8. Relative Luminous Intensity as a function of case temperature at fixed current level.

Solid State Plus/Minus Sign

For display applications requiring ± designation, the 5082-7018 solid state plus/minus sign is available. This display module comes in the same package as the 5082-7000 numeric indicator and is completely compatible with it. Plus or minus information can be indicated by supplying voltage to one (minus sign) or two (plus sign) input leads. A third lead is provided for the ground connection. Brightness is variable by changing the dc drive voltage. Like the numeric indicator, the 7018 plus/minus sign is completely IC compatible, small in size, and rugged in design.

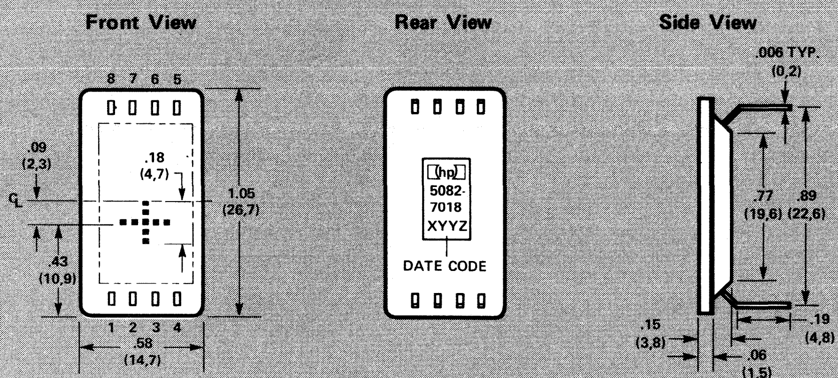
Truth Table

CHARACTER	PIN	
	3	7
+	H	H
–	L	H
Blank	L	L

Note: L = –0.5 to 1.0V
H = 2.5 to 4.2V

Package Dimensions

5082-7018 Plus/Minus Sign



FUNCTION/PIN	
NC	1
NC	2
Plus	3
NC	4
NC	5
Ground	6
Minus/Plus	7
NC	8

Absolute Maximum Ratings

Description	Symbol	Min.	Max.	Unit
Storage Temperature, Ambient	T_S	–65	+100	°C
Operating Temperature, Case	T_C	–55	+95	°C
Plus, Plus/Minus Input Potential to Ground	V_{LED}	–0.5	4.2	V

Recommended Operating Conditions

Description	Symbol	Min.	Nom.	Max.	Unit
LED Supply Voltage, Display Off	V_{LED}	–0.5	0	1.0	V
LED Supply Voltage, Display On	V_{LED}	2.5	4.0	4.2	V

Electrical/Optical Characteristics (T_C = 0°C to 70°C, unless otherwise specified)

Description	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
LED Supply Current	I_{LED}	V_{LED} = 4.2V		100	150	mA
Power Dissipation	P_T	V_{LED} = 4.2V		0.4	0.6	W
Luminous Intensity per LED (Digit Average)	I_v	V_{LED} = 4.2V [1]	40	100		μcd
Luminous Intensity per LED (Digit Average)	I_v	V_{LED} = 3.5V [1]		50		μcd
Peak Wavelength	λ_{peak}	T_C = 25°C		655		nm
Spectral Halfwidth	$\Delta\lambda_{1/2}$	T_C = 25°C		30		nm
Weight				3.1		gram

NOTE 1: T_C = 25°C.

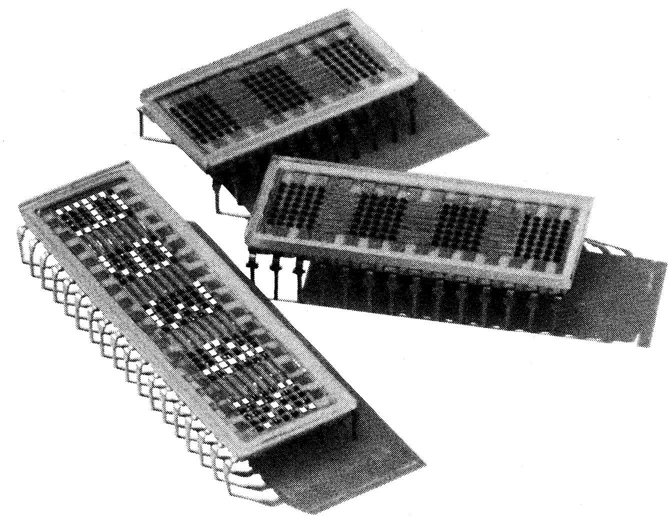
HEWLETT hp PACKARD
COMPONENTS

LED SOLID STATE ALPHANUMERIC INDICATOR

5082-7100 5082-7101 5082-7102

Features

- 5 x 7 LED Matrix Character
  - Human Factors Engineered
- Brightness Controllable
- IC Compatible
- Small Size
  - Standard .600 inch Dual In-Line Package
  - .27 inch Character Height
- Wide Viewing Angle
- Rugged, Shock Resistant
  - Hermetically Sealed
  - Designed to Meet MIL Standards
- Long Operating Life



Description

The Hewlett-Packard 5082-7100 Series is an X-Y addressable, 5 x 7 LED Matrix capable of displaying the full alphanumeric character set. This alphanumeric indicator series is available in 3, 4, or 5 character end-stackable clusters. The clusters permit compact presentation of information, ease of character alignment, minimum number of interconnections, and compatibility with multiplexing driving schemes.

Alphanumeric applications include computer terminals, calculators, military equipment and space flight readouts.

The **5082-7100** is a three character cluster.
The **5082-7101** is a four character cluster.
The **5082-7102** is a five character cluster.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Peak Forward Current Per LED (Duration < 1 ms)	I_{peak}		100	mA
Average Current Per LED	I_{AVG}		10	mA
Power Dissipation Per Character (All diodes lit)[1]	P_D		700	mW
Operating Temperature, Case	T_C	–55	95	°C
Storage Temperature	T_S	–55	100	°C
Reverse Voltage Per LED	V_R		4	V

Note 1: At 25°C Case Temperature; derate 8.5 mW/°C above 25°C.

Electrical / Optical Characteristics at $T_C = 25°C$

Parameter	Symbol	Min.	Typ.	Max.	Units
Peak Luminous Intensity Per LED (Character Average) @ Pulse Current of 100mA/LED	$I_{v\ (peak)}$	1.0	2.2		mcd
Reverse Current Per LED @ V_R = 4V	I_R			10	μA
Peak Forward Voltage @ Pulse Current of 100mA/LED	V_F		1.7	2.0	V
Peak Wavelength	λ_{peak}		655		nm
Spectral Line Halfwidth	$\Delta\lambda_{1/2}$		30		nm
Rise and Fall Times [1]	t_r, t_f		10		ns

Note 1. Time for a 10% - 90% change of light intensity for step change in current.

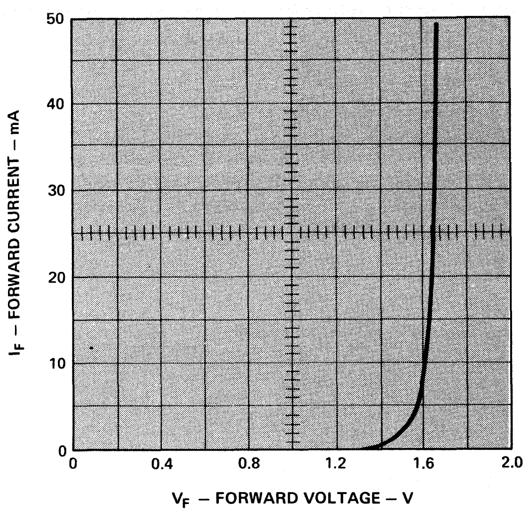


Figure 1. Forward Current-Voltage Characteristic.

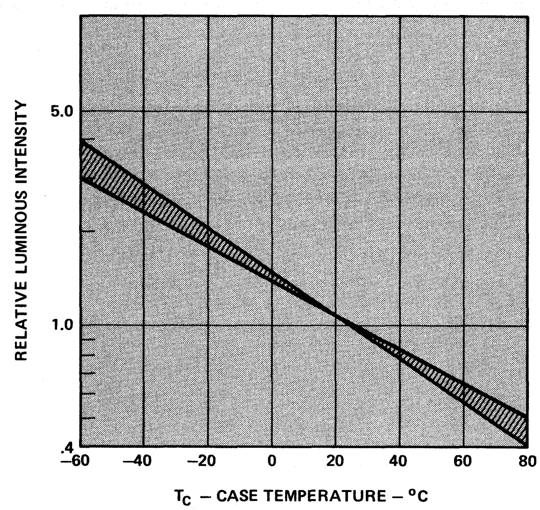


Figure 2. Relative Luminous Intensity vs. Case Temperature at Fixed Current Level.

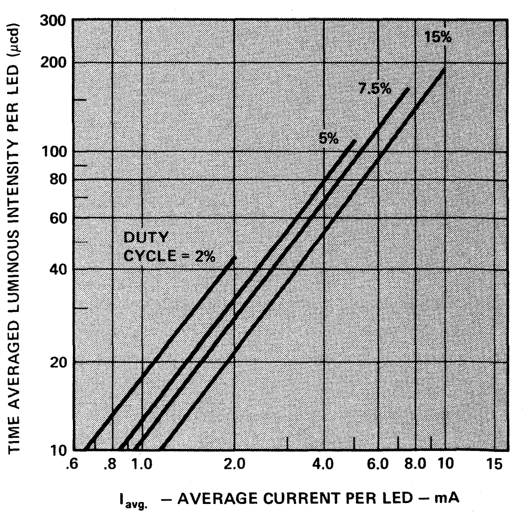


Figure 3. Typical Time Averaged Luminous Intensity per LED vs. Average Current per LED.

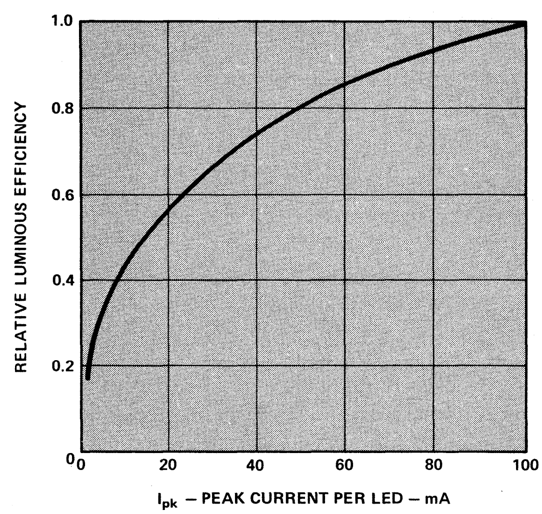
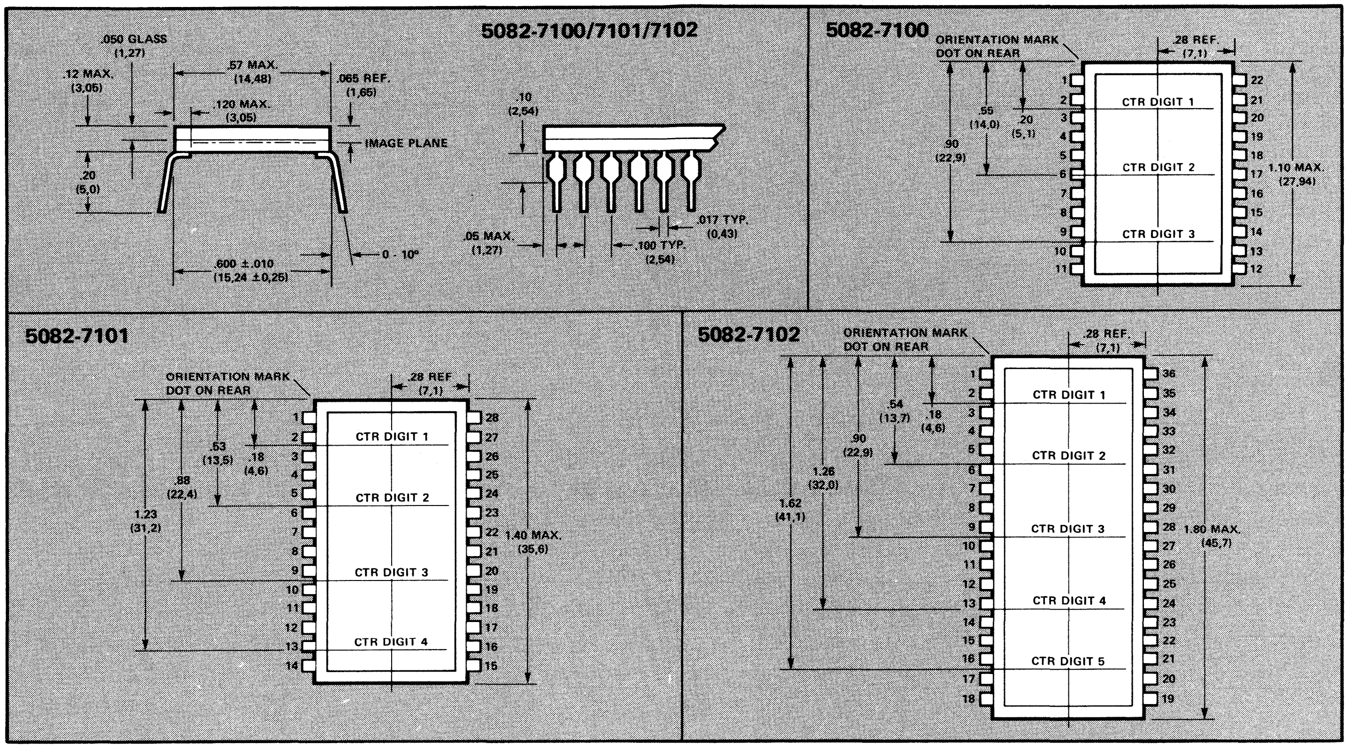


Figure 4. Typical Relative Luminous Efficiency vs. Peak Current per LED.

Package Dimensions and Pin Configurations



Notes:
1. Dimensions are in inches and (millimeters).
2. Unless otherwise specified, the tolerance on all dimensions is ±.015 inches (±0,38mm).
3. Character Size .27 x .19 inches (6, 9 x 4, 9mm).

Device Pin Description

5082-7100

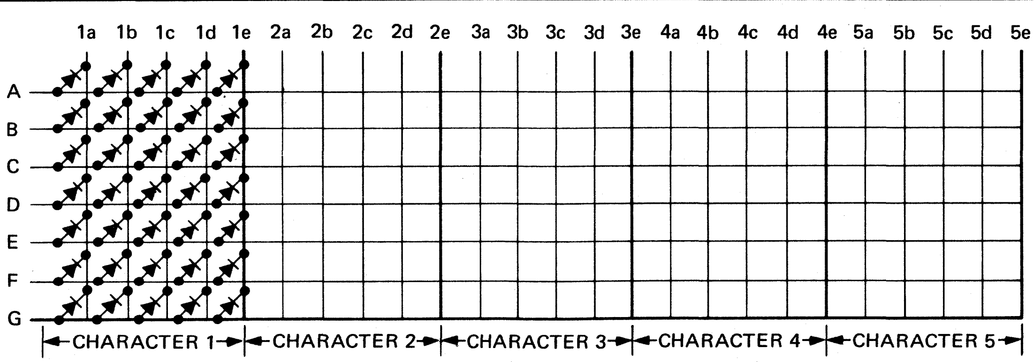
Pin	Function	Pin	Function
1	Anode G	12	Anode B
2	1c	13	3d
3	1d	14	3b
4	Anode F	15	Anode A
5	Anode E	16	2e
6	2b	17	2c
7	2d	18	2a
8	Anode C	19	Anode D
9	3a	20	1e
10	3c	21	1b
11	3e	22	1a

5082-7101

Pin	Function	Pin	Function
1	N/C	15	Anode C
2	1c	16	4c
3	1e	17	4a
4	Anode G	18	Anode B
5	2b	19	3e
6	2d	20	3b
7	Anode D	21	3a
8	Anode E	22	2e
9	3c	23	2c
10	3d	24	2a
11	Anode F	25	Anode A
12	4b	26	1d
13	4d	27	1b
14	4e	28	1a

5082-7102

Pin	Function	Pin	Function
1	N/C	19	5e
2	1c	20	5c
3	1e	21	5a
4	Anode F	22	Anode D
5	2b	23	4e
6	2d	24	4c
7	2e	25	N/C
8	Anode E	26	Anode C
9	3c	27	3d
10	3e	28	3b
11	Anode G	29	3a
12	4a	30	Anode B
13	4b	31	2c
14	4d	32	2a
15	N/C	33	Anode A
16	5b	34	1d
17	5d	35	1b
18	N/C	36	1a



5082-7100/7101/7102 Schematic Wiring Diagram

Operating Considerations

ELECTRICAL

The 5 x 7 matrix of LED's, which make up each character, are X-Y addressable. This allows for a simple addressing, decoding and driving scheme between the display module and customer furnished logic.

There are three main advantages to the use of this type of X-Y addressable array:

1. It is an elementary addressing scheme and provides the least number of interconnection pins for the number of diodes addressed. Thus, it offers maximum flexibility toward integrating the display into particular applications.
2. This method of addressing offers the advantage of sharing the Read-Only-Memory character generator among several display elements. One character generating ROM can be shared over 25 or more 5 x 7 dot matrix characters with substantial cost savings.
3. In many cases equipments will already have a portion of the required decoder/driver (timing and clock circuitry plus buffer storage) logic circuitry available for the display.

To form alphanumeric characters a method called "scanning" or "strobing" is used. Information is addressed to the display by selecting one row of diodes at a time, energizing the appropriate diodes in that row and then proceeding to the next row. After all rows have been excited one at a time, the process is repeated. By scanning through all rows at least 100 times a second, a flicker free character can be produced. When information moves sequentially from row to row of the display (top to bottom) this is vertical scanning, as illustrated in Figure 5. Information can also be moved from column to column (left to right across the display) in a horizontal scanning mode. For most applications (5 or more characters to share the same ROM) it is more economical to use vertical scanning.

A much more detailed description of general scanning techniques along with specific circuit recommendations is contained in HP Application Note 931.

MECHANICAL/THERMAL MOUNTING

The solid state display typically operates with 200mW power dissipation per character. However, if the operating conditions are such that the power dissipation exceeds the derated maximum allowable value, the device should be heat sunk. The usual mounting technique combines mechanical support and thermal heat sinking in a common structure. A metal strap or bar can be mounted behind the display using silicone grease to insure good thermal control. A well-designed heat sink can limit the case temperature to within 10°C of ambient.

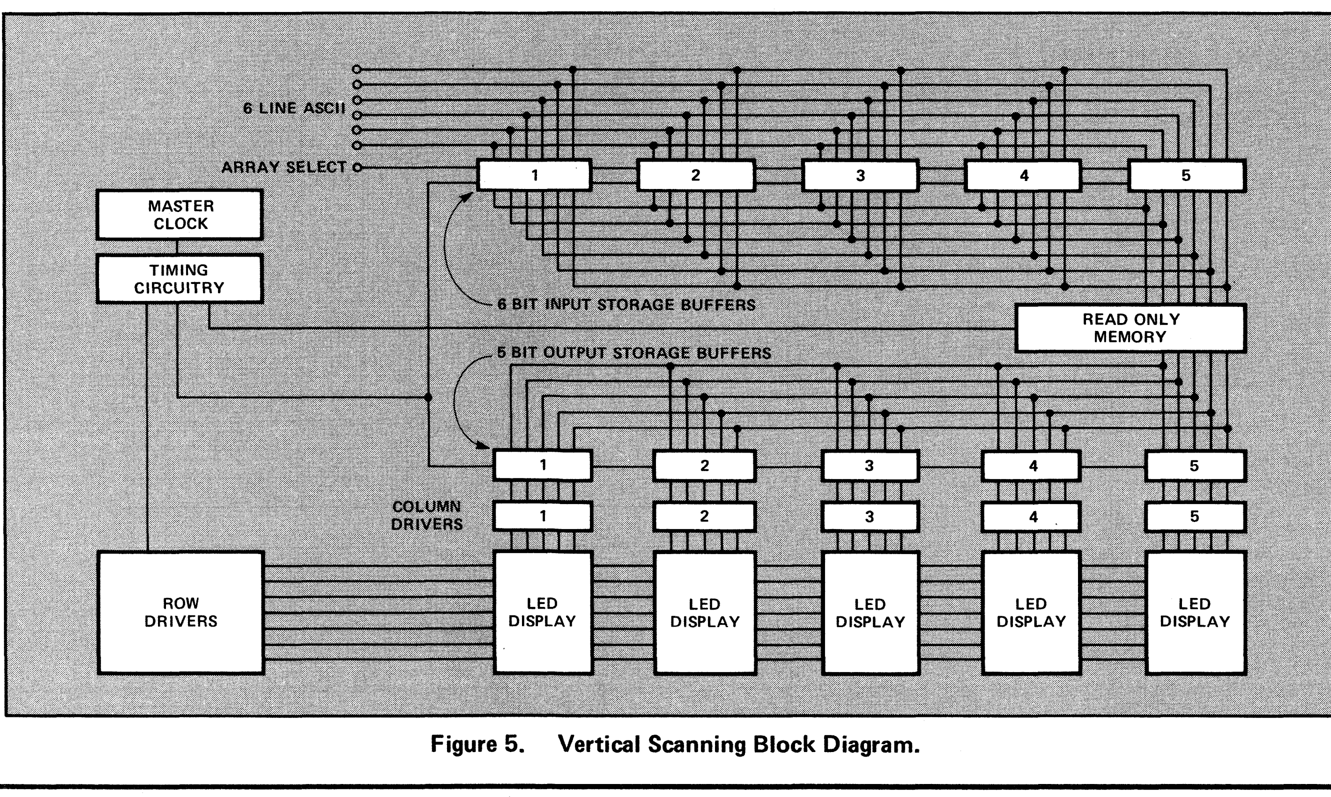


Figure 5. Vertical Scanning Block Diagram.

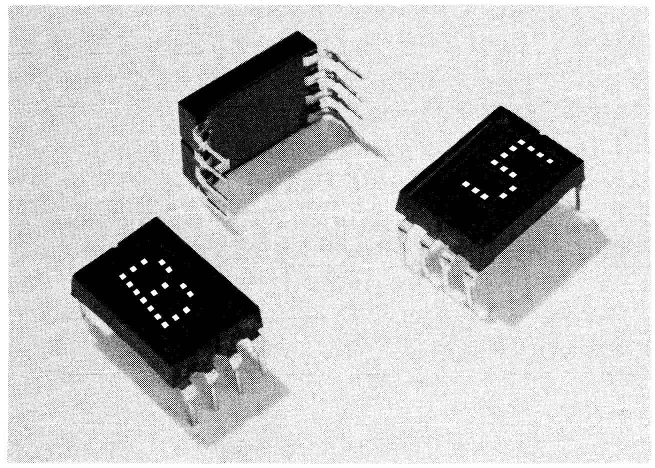
HEWLETT hp PACKARD
COMPONENTS

NUMERIC and HEXADECIMAL INDICATORS

5082-7300 SERIES

FEATURES

- Numeric 5082-7300/-7302
  - 0-9, Test State, Minus Sign, Blank States
  - Decimal Point
    - 7300 Right Hand D.P.
    - 7302 Left Hand D.P.
- Hexadecimal 5082-7340
  - 0-9, A-F, Base 16 Operation
  - Blanking Control, Conserves Power
  - No Decimal Point
- DTL — TTL Compatible
- Includes Decoder/Driver with Memory
  - 8421 Positive Logic Input
- 4 X 7 Dot Matrix Array
  - Shaped Character, Excellent Readibility
- Standard .600 inch X .400 inch Dual-in-Line Package including Contrast Filter
- Categorized for Luminous Intensity
  - Assures Uniformity of Light Output from Unit to Unit within a Single Category

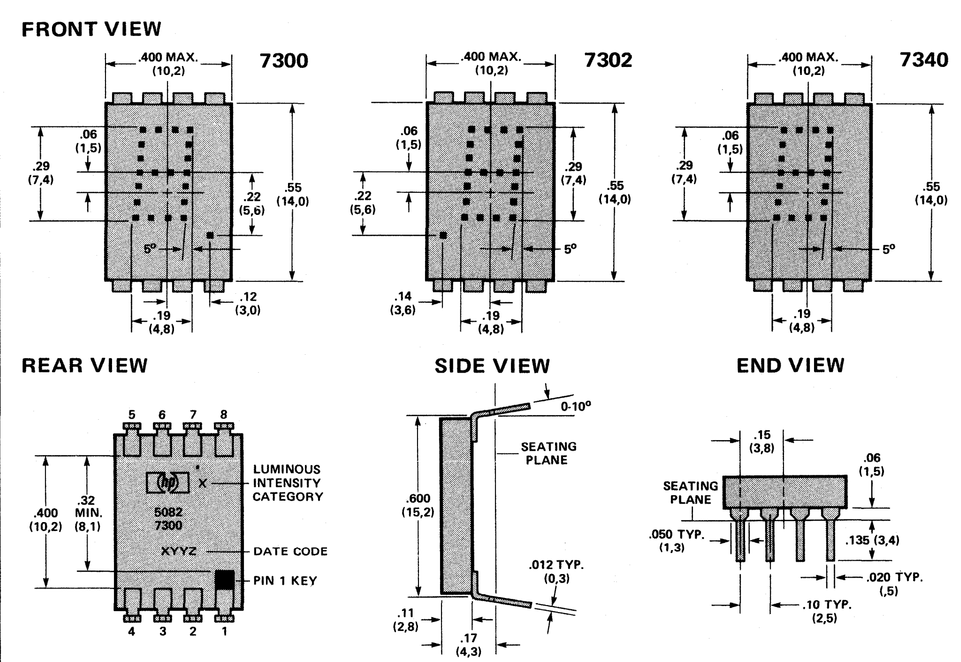


DESCRIPTION

The HP 5082-7300 series solid state numeric and hexadecimal indicators with on-board decoder/driver and memory provide a reliable, low-cost method for displaying digital information.
The 5082-7300 numeric indicator decodes positive 8421 BCD logic inputs into characters 0-9, a "-" sign, a test pattern, and four blanks in the invalid BCD states, The unit employs a right-hand decimal point. Typical applications include point-of-sale terminals, instrumentation, and computer systems.

The 5082-7302 is the same as the 5082-7300, except that the decimal point is located on the left-hand side of the digit.
The 5082-7340 hexadecimal indicator decodes positive 8421 logic inputs into 16 states, 0-9 and A-F. In place of the decimal point an input is provided for blanking the display (all LED's off), without losing the contents of the memory. Applications include terminals and computer systems using the base-16 character set.
The 5082-7304 is a "±1" overrange character, including decimal point, used in instrumentation applications.

PACKAGE DIMENSIONS



PIN	FUNCTION: 5082-7300 and 7302 Numeric	FUNCTION: 5082-7340 Hexadecimal
1	Input 2	Input 2
2	Input 4	Input 4
3	Input 8	Input 8
4	Decimal point	Blanking control
5	Latch enable	Latch enable
6	Ground	Ground
7	V_{CC}	V_{CC}
8	Input 1	Input 1

NOTES:
1. Dimensions in inches and (millimeters).
2. Unless otherwise specified, the tolerance on all dimensions is ± .015"(±,38mm).
3. Vertical digit center line is ±.02" (±,51mm) from vertical package center line.

ABSOLUTE MAXIMUM RATINGS

DESCRIPTION	SYMBOL	MIN	MAX	UNIT
Storage temperature, ambient	T_S	-40	+100	°C
Operating temperature, case	T_C	-20	+85	°C
V_{cc} Pin potential to ground pin	V_{cc}	-0.5	+7.0	V
Voltage applied to input logic pins and decimal point (1)	V_{in}	-0.5	+5.5	V
Voltage applied to latch enable	V_E	-0.5	+5.5	V
Voltage applied to blanking control (2)	V_B	-0.5	+5.5	V

NOTES: 1. Decimal point applies only to 7300/7302 2. Applies only to 7340

RECOMMENDED OPERATING CONDITIONS

DESCRIPTION	SYMBOL	MIN	NOM	MAX	UNIT
Supply Voltage	V_{cc}	4.5	5.0	5.5	V
Logic voltage "0" state	$V_{in(0)}$	0		0.8	V
Logic voltage "1" state	$V_{in(1)}$	2.0		5.25	V
Latch enable voltage-date being entered	$V_{E(0)}$	0		0.8	V
Latch enable voltage-data not being entered	$V_{E(1)}$	2.0		5.25	V
Blanking control voltage-display not blanked (1)	$V_{B(0)}$	0		0.8	V
Blanking control voltage-display blanked (1)	$V_{B(1)}$	3.5		5.25	V

NOTE: 1. Applies only to 7340

ELECTRICAL/OPTICAL CHARACTERISTICS (T_C = -20°C to +85°C, unless otherwise specified)

DESCRIPTION	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply current	I_{cc}	V_{cc} = 5.5V		94(1)	170(2)	mA
Power dissipation	P_T	V_{cc} = 5.5V		470(1)	935(2)	mW
Luminous intensity per LED (Digit average) (3)	I_ν	V_{cc} = 5.0V, T_C = 25°C	32	70		μcd
Minimum time data must be presented to logic input prior to enable rising	t_{setup}	V_{cc} = 5.0V, $V_{E(0)}$ = 0.4V $V_{in(0)}$ = 0.4V, $V_{E(1)}$ = 2.4V $V_{in(1)}$ = 2.4V, T_C = 25°C		30	50	ns
Minimum time data must be held after enable rises	t_{hold}	V_{cc} = 5.0V, $V_{E(0)}$ = 0.4V $V_{in(0)}$ = 0.4V, $V_{E(1)}$ = 2.4V $V_{in(1)}$ = 2.4V, T_C = 25°C		30	50	ns
Time required for 90% change in display luminous intensity after change of state of V_B (4)	t_{blank}	V_{cc} = 5.0V, T_C = 25°C			500	ns
Blanking control current "0" state (4)	$I_{B(0)}$	V_{cc} = 5.5V, $V_{B(0)}$ = 0.8V			200	μA
Blanking control current "1" state (4)	$I_{B(1)}$	V_{cc} = 5.5V, $V_{B(1)}$ = 4.5V			2.0	mA
Logic and latch enable currents "0" state	$I_{in(0)}$, $I_{E(0)}$	V_{cc} = 5.5V V_{in}, V_E = 0.4V			-1.6	mA
Logic and latch enable currents "1" state	$I_{in(1)}$, $I_{E(1)}$	V_{cc} = 5.5V V_{in}, V_E = 2.4V			+250	μA
Peak wavelength	λ_{peak}	T_C = 25°C		655		nm
Spectral halfwidth	$\Delta\lambda_{1/2}$	T_C = 25°C		30		nm
Weight				0.8		gm

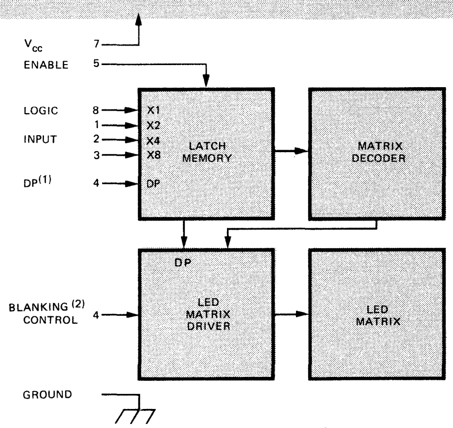
NOTES:
1. V_{cc} = 5.0V with statistical average number of LED's lit.
2. Worst case condition excluding test state on 5082-7300/-7302.
3. The digits are categorized for luminous intensity such that the variation from digit to digit within a category is not discernible to the eye. Intensity categories are designated by a letter located on the reverse side of the package contiguous with the Hewlett-Packard logo marking.
4. Applies only to 7340.

TRUTH TABLE FOR 5082-7300 SERIES DEVICES

CHARACTER		INPUTS						CHARACTER		INPUTS					
5082–7300/7302 Numeric	5082–7340 Hex.	X8	X4	X2	X1	E	B(1)	5082-7300/7302 NUMERIC	5082–7340 Hex.	X8	X4	X2	X1	E	B(1)
0	0	L	L	L	L	L	L	Test	A	H	L	H	L	L	L
1	1	L	L	L	H	L	L	Blank	B	H	L	H	H	L	L
2	2	L	L	H	L	L	L	Blank	C	H	H	L	L	L	L
3	3	L	L	H	H	L	L	Minus	D	H	H	L	H	L	L
4	4	L	H	L	L	L	L	Blank	E	H	H	H	L	L	L
5	5	L	H	L	H	L	L	Blank	F	H	H	H	H	L	L
6	6	L	H	H	L	L	L	Hold	Hold	d	d	d	d	H	d
7	7	L	H	H	H	L	L	—	Blank (1)	d	d	d	d	d	H
8	8	H	L	L	L	L	L	Decimal pt. on (2)	—	DP_{in} = L					
9	9	H	L	L	H	L	L	Decimal pt. off (2)	—	DP_{in} = H					

NOTES:

1. The blanking control input, B, pertains to the 5082-7340 Hexadecimal Indicator only.
2. The decimal point input pertains to the 5082-7300 and -7302 Numeric Indicators only.
3. H = logic '1'; L = logic '0'; d = 'don't care'.



Notes 1. 5082 — 7300/-7302 only
2. 5082 — 7340 only

Figure 1. Block Diagram of 5082-7300 Series Logic.

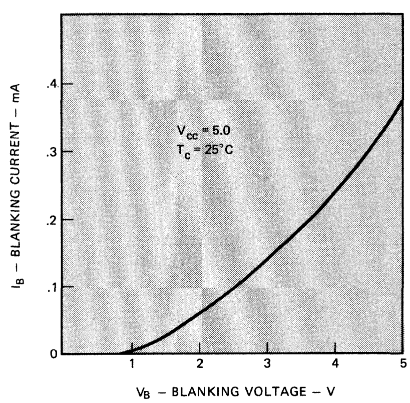


Figure 2. Typical Blanking Control Current Vs. Voltage for 5082-7340 Only.

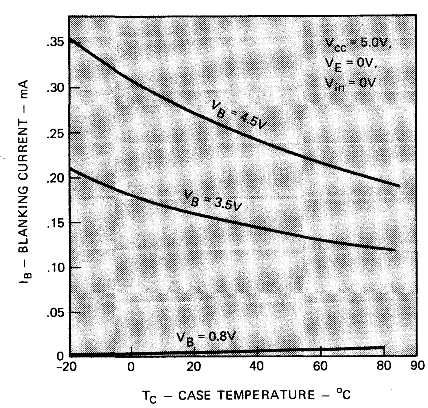


Figure 3. Typical Blanking Control Input Current Vs. Temperature, 5082-7340.

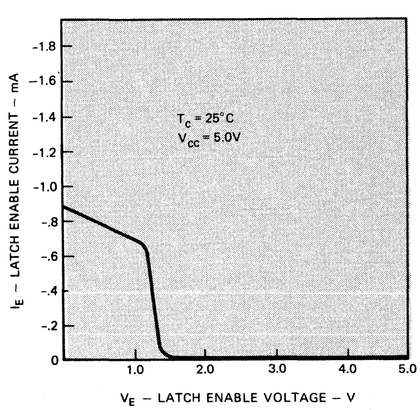


Figure 4. Typical Latch Enable Input Current Vs. Voltage for the 5082-7300 Series Devices.

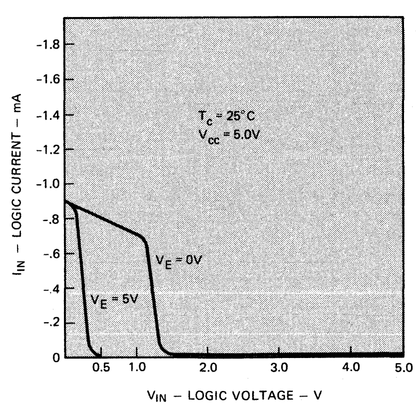


Figure 5. Typical Logic and Decimal Point Input Current Vs. Voltage for the 5082-7300 Series Devices. Decimal Point Applies to 5082-7300 Only.

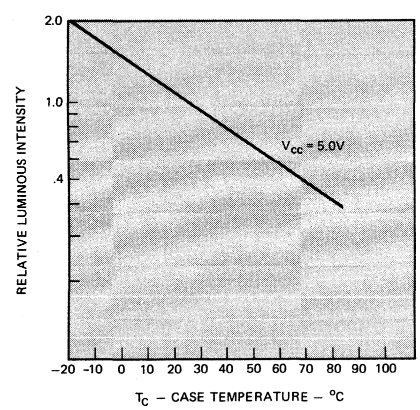


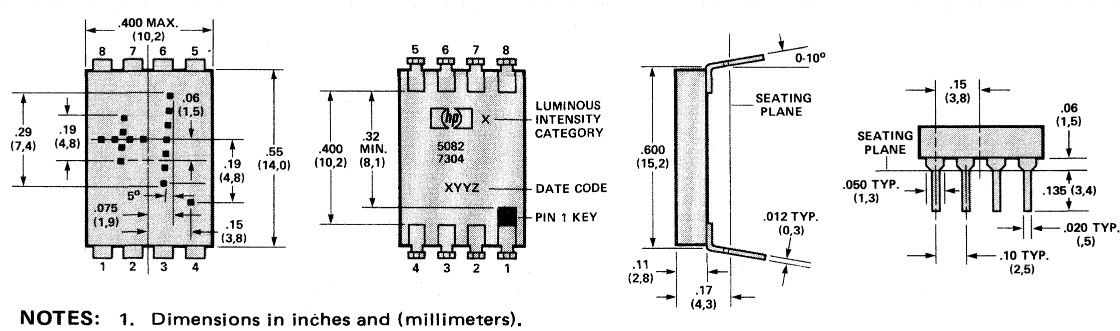
Figure 6. Typical Luminous Intensity Vs. Case Temperature for the 5082-7300 Series Devices.

SOLID STATE OVER RANGE CHARACTER

For display applications requiring a ±, 1, or decimal point designation, the 5082-7304 over range character is available. This display module comes in the same package as the 5082-7300 series numeric indicator and is completely compatible with it.

PACKAGE DIMENSIONS

FRONT VIEW **REAR VIEW** **SIDE VIEW** **END VIEW**



PIN	FUNCTION
1	Plus
2	Numeral One
3	Numeral One
4	DP
5	Open
6	Open
7	V_{CC}
8	Minus/Plus

NOTES: 1. Dimensions in inches and (millimeters).
2. Unless otherwise specified, the tolerance on all dimensions is ±.015 inches. (± ,38mm)

5082–7304

TRUTH TABLE FOR 5082-7304

CHARACTER	PIN			
	1	2,3	4	8
+	1	d	d	1
–	0	d	d	1
1	d	1	d	d
Decimal Point	d	d	1	d
Blank	0	0	0	0

NOTES: 0: Line switching transistor in Fig. 7 cutoff.
1: Line switching transistor in Fig. 7 saturated.
d: 'don't care'

TYPICAL DRIVING CIRCUIT FOR 5082-7304.

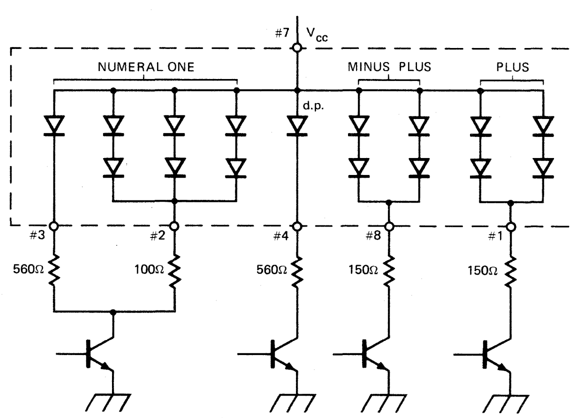


Figure 7.

ABSOLUTE MAXIMUM RATINGS

DESCRIPTION	SYMBOL	MIN	MAX	UNIT
Storage temperature, ambient	T_s	-40	+100	°C
Operating temperature, case	T_C	-20	+85	°C
Forward current, each LED	I_F		10	mA
Reverse voltage, each LED	V_R		4	V

RECOMMENDED OPERATING CONDITIONS

	SYMBOL	MIN	NOM	MAX	UNIT
LED supply voltage	V_{CC}	4.5	5.0	5.5	V
Forward current, each LED	I_F		5.0	10	mA

NOTE:
LED current must be externally limited. Refer to figure 7 for recommended resistor values.

ELECTRICAL/OPTICAL CHARACTERISTICS (T_C = -20°C TO +85°C, UNLESS OTHERWISE SPECIFIED)

DESCRIPTION	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Forward Voltage per LED	V_F	I_F = 10 mA		1.6	2.0	V
Power dissipation	P_T	I_F = 10 mA all diodes lit		250	320	mW
Luminous Intensity per LED (digit average)	I_v	I_F = 6 mA T_C = 25°C	32	70		μcd
Peak wavelength	λ_{peak}	T_C = 25°C		655		nm
Spectral halfwidth	$\Delta\lambda_{1/2}$	T_C = 25°C		30		nm
Weight				0.8		gm

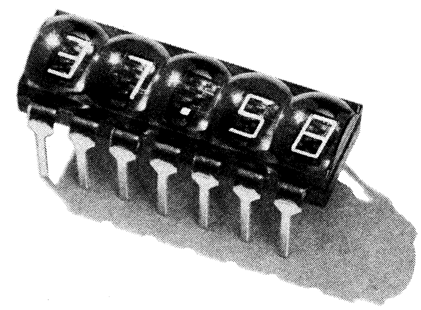
HEWLETT PACKARD
COMPONENTS

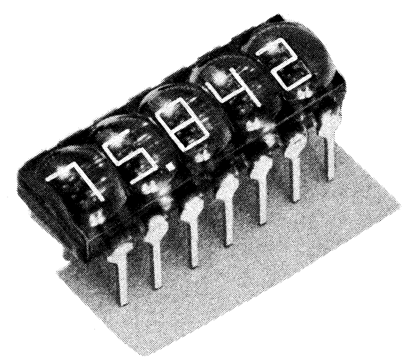
SOLID STATE NUMERIC INDICATOR (7 Segment Monolithic)

5082-7400 SERIES

Features

- Ultra Low Power
  - Excellent Readibility at Only 1 mW per Segment
- Constructed for Stobed Operation
  - Minimizes Lead Connections
- Standard DIP Package
  - End Stackable
  - Integral Red Contrast Filter
  - Rugged Construction
- Categorized for Luminous Intensity
  - Assures Uniformity of Light Output from Unit to Unit within a Single Category
- IC Compatible



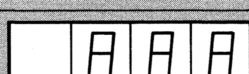
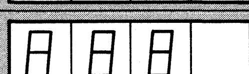
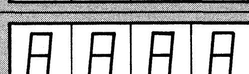


Description

The HP 5082-7400 series are .11 inch high, seven segment GaAsP numeric indicators packaged in 3, 4, and 5 digit end-stackable clusters. An integral magnification technique increases the luminous intensity, thereby making ultra-low power consumption possible. Options include either the standard lower right hand decimal point or a centered decimal point for increased legibility in multi-cluster applications.

Applications include hand-held calculators, portable instruments, digital thermometers, or any other product requiring low power, low cost, minimum space, and long lifetime indicators.

Device Selection Guide

Digits per Cluster	Configuration		Part Number	
	Device	Package	Center Decimal Point (Figure 7)	Right Decimal Point (Figure 8)
3 (right)		(Figure 5)	5082-7402	5082-7412
3 (left)		(Figure 5)	5082-7403	5082-7413
4		(Figure 5)	5082-7404	5082-7414
5		(Figure 6)	5082-7405	5082-7415

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Peak Forward Current per Segment (Duration < 1 msec)	I_{PEAK}		110	mA
Average Current per Segment	I_{AVG}		5	mA
Power Dissipation per Digit [1]	P_D		80	mW
Operating Temperature, Ambient	T_A	–40	75	°C
Storage Temperature	T_S	–40	100	°C
Reverse Voltage	V_R		5	V

Note 1: At 25°C; derate 1 mW/°C above 25°C ambient.

Electrical/Optical Characteristics at T_A=25°C

Parameter	Symbol	Min.	Typ.	Max.	Units
Peak Forward Voltage per Segment @ Peak Current of 80mA/seg.	V_F		1.7	2.0	V
Peak Luminous Intensity per Segment @ Peak Current of 80mA/seg. [1]	$I_{\nu\,(peak)}$	0.4	2.6		mcd
Reverse Current per Segment @ V_R = 5V	I_R			100	μA
Peak Wavelength			655		nm
Rise and Fall Time [2]	t_r, t_f		10		ns

Note 1. The digits are categorized for luminous intensity such that the variation from digit to digit within a category is not discernible to the eye. Intensity categories are designated by a letter located on the reverse side of the package.

Note 2. Time for a 10%-90% change of light intensity for step change in current.

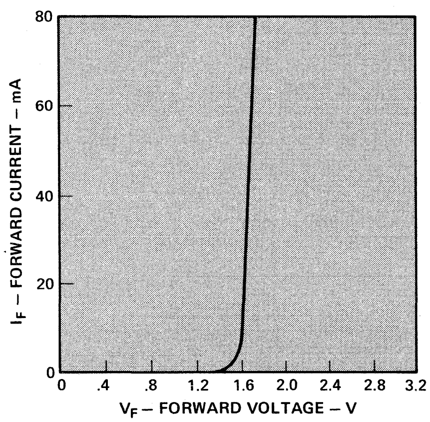


Figure 1. Forward Current vs. Forward Voltage.

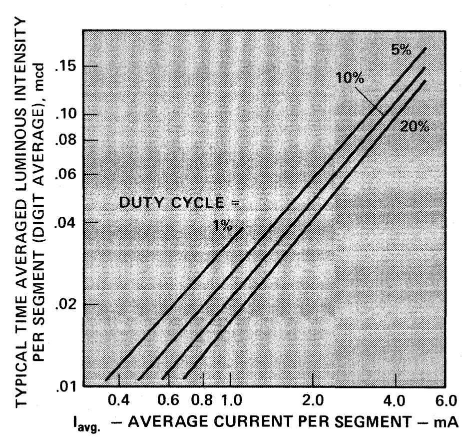


Figure 2. Typical Time Averaged Luminous Intensity per Segment (Digit Average) vs. Average Current per Segment.

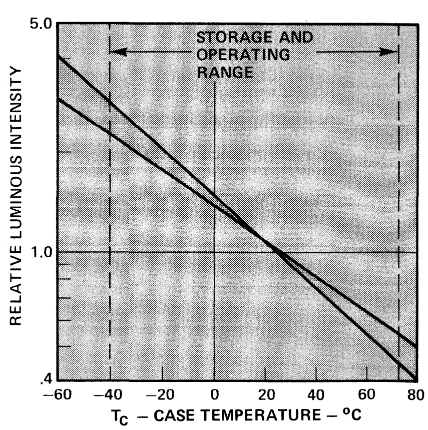


Figure 3. Relative Luminous Intensity vs. Case Temperature at Fixed Current Level.

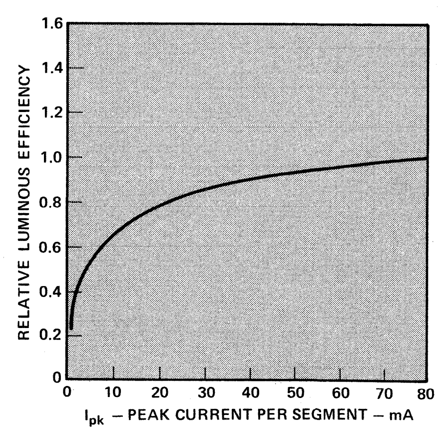


Figure 4. Relative Luminous Efficiency vs. Peak Current per Segment.

Package Description

Note 1. Dimensions in inches and (millimeters)
Note 2. Tolerances on all dimensions are ±.015 (0,038) unless otherwise noted.

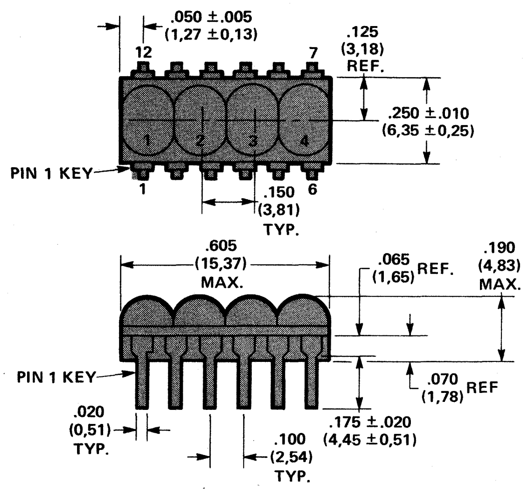


Figure 5. 5082-7402/-7403/-7404/ -7412/-7413/-7414

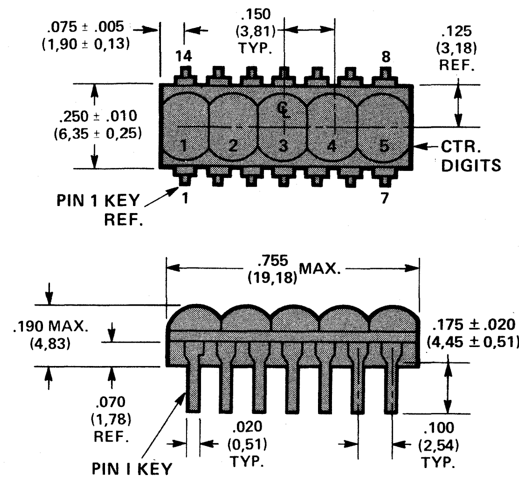
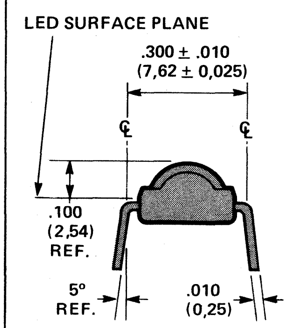


Figure 6. 5082-7405/7415



All Devices

Magnified Character Font Description

DEVICES
5082-7402
5082-7403
5082-7404
5082-7405

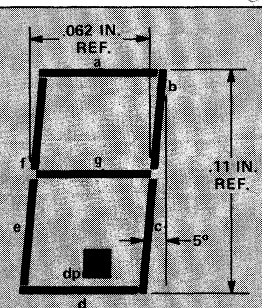


Figure 7. Center Decimal Point Configuration.

DEVICES
5082-7412
5082-7413
5082-7414
5082-7415

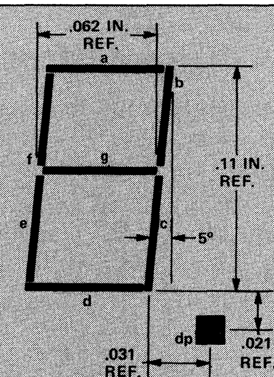


Figure 8. Right Decimal Point Configuration

Device Pin Description

PIN NO.	5082-7402/7412 FUNCTION	5082-7403/7413 FUNCTION	5082-7404/7414 FUNCTION	5082-7405/7415 FUNCTION
1	N/C	CATHODE 1	CATHODE 1	CATHODE 1
2	ANODE e	ANODE e	ANODE e	ANODE e
3	ANODE c	ANODE c	ANODE c	ANODE c
4	CATHODE 3	CATHODE 3	CATHODE 3	CATHODE 3
5	ANODE dp	ANODE dp	ANODE dp	ANODE dp
6	CATHODE 4	N/C	CATHODE 4	ANODE d
7	ANODE g	ANODE g	ANODE g	CATHODE 5
8	ANODE d	ANODE d	ANODE d	ANODE g
9	ANODE f	ANODE f	ANODE f	CATHODE 4
10	CATHODE 2	CATHODE 2	CATHODE 2	ANODE f
11	ANODE b	ANODE b	ANODE b	(See Note 1)
12	ANODE a	ANODE a	ANODE a	ANODE b
13	–	–	–	CATHODE 2
14	–	–	–	ANODE a

Note 1. Leave Pin 11 unconnected.

Electrical

Character encoding can be performed by commercially available BCD-7 segment decoder/driver circuits. Through the use of a strobing technique, only one decoder/driver is required for each display. In addition, the number of interconnection lines between the display and the drive circuitry is minimized to 8 + N, where N is the number of characters in the display.

Each of the segments on the display is "addressable" on two sets of lines – the "character enable" lines and the "segment enable" lines. Displays are wired so that all of the cathodes of all segments comprising one character are wired together to a single character enable line. Similarly, the anodes of each of like segments (e.g., all of the decimal points, all of the center line anodes, etc.) are wired to a single line. Therefore, a single digit in the cluster can be illuminated by connecting the appropriate character enable line, with the appropriate segment enable lines for the character being displayed. When each character in the display is illuminated in sequence, at a minimum of 100 times a second, flicker free characters are formed.

The decimal point in the 7412, 7413, 7414, and 7415 displays is located at the lower right of the digit for conventional driving schemes.

The 7402, 7403, 7404 and 7405 displays contain a centrally located decimal point which is activated in place of a digit. In long registers, this technique of setting off the decimal point significantly improves the display's readability. With respect to timing, the decimal point is treated as a separate character with its own unique time frame.

A detailed discussion of display circuits and drive techniques appears in Application Note 937.

Mechanical

The 5082-7400 series package is a standard 12 or 14 Pin DIP consisting of a plastic encapsulated lead frame with integral molded lenses. It is designed for plugging into DIP sockets or soldering into PC boards. The lead frame construction allows use of standard DIP insertion tools and techniques. Alignment problems are simplified due to the clustering of digits in a single package. The shoulders of the lead frame pins are intentionally raised above the bottom of the package to allow tilt mounting of up to 20° from the PC board.

To improve display contrast, the plastic incorporates a red dye that absorbs strongly at all visible wavelengths except the 655 nm emitted by the LED. In addition, the lead frames are selectively darkened to reduce reflectance. An additional filter, such as Plexiglass 2423, will further lower the ambient reflectance and improve display contrast.

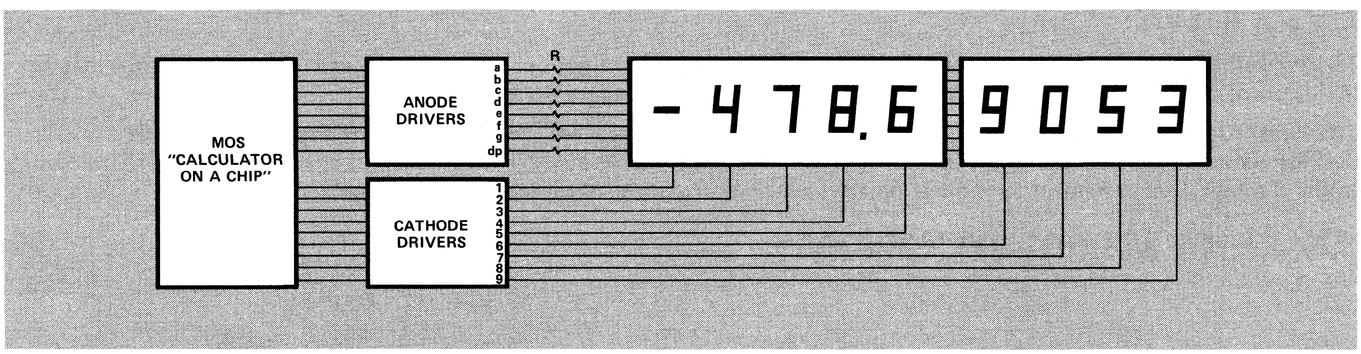


Figure 9. Block Diagram for Calculator Display Using Lower Right Hand Decimal Point.

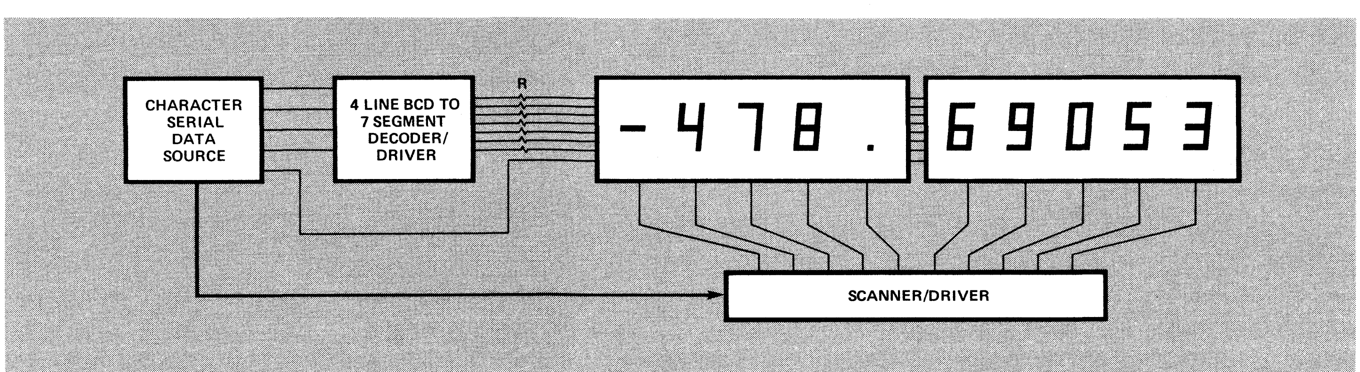
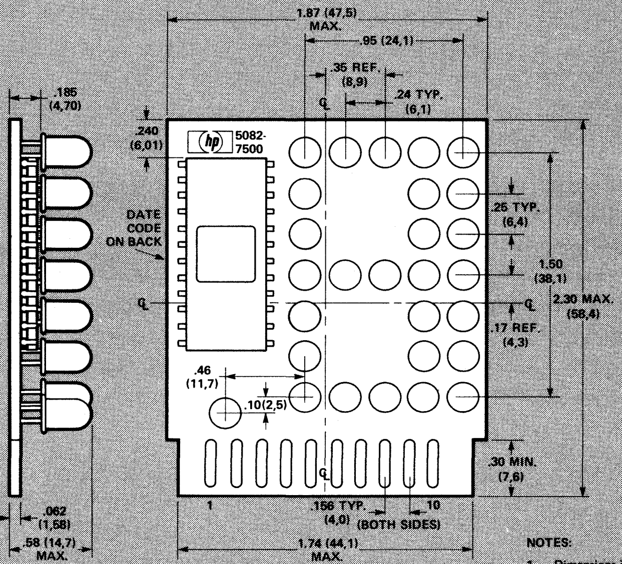


Figure 10. Block Diagram for Display Using Center Decimal Point.

HEWLETT hp PACKARD
COMPONENTS

SOLID STATE NUMERIC 1.5" INDICATOR

5082-7500



PIN	FUNCTION
1	V_{CC}
2	DP
3	X1
4	X2
5	X4
6	X8
7	GROUND
8	NC
9	NC
10	V_{LED}

NOTES:
1. Dimensions in inches and (millimeters).
2. Unless otherwise specified, the tolerance on all dimensions is ±.015 inches (±0,38mm).

Features

- 1.5 Inch High Character
  - Readable From 60 Feet
- On-Board Decoder/Driver
  - 8421 Positive Logic Input
  - DTL-TTL Compatible
- 5 x 7 Dot Matrix
  - Shaped Character For Excellent Readability
- Single Plane Construction
  - Wide Viewing Angle
- Edge Mounting in Standard PC Board Connectors (.156" centers)
- Reliable, Rugged, Long Operating Life

Description

The HP 5082-7500 is a 1.5" numeric indicator utilizing discrete red light emitting diodes arranged in a 5 x 7 dot matrix. Inclusion of the decoder/driver permits direct addressing by the standard BCD code.

The large size and high efficiency light emitters permit viewing distances up to 60 feet. The single plane of light emitters permits wide viewing angles and low mounting space requirements. Applications include equipment for scales, process control and medical measurement, and other data systems requiring ease of readability at a distance.

Absolute Maximum Ratings

Description	Symbol	Min.	Max.	Unit
Storage Temperature, Ambient	T_S	–40	85	°C
Operating Temperature, Ambient	T_A	–20	70	°C
Logic Supply Voltage [1]	V_{CC}	–0.5	7	V
LED Supply Voltage [1, 2]	V_{LED}	–0.5	5.25	V
Voltage Applied to BCD [1, 2] and Decimal Point Inputs	V_{in}	–0.5	5.25	V

[1] Voltage values are with respect to ground pin. [2] V_{in} or V_{LED} not to exceed V_{CC} by more than 0.5V at any time.

Recommended Operating Conditions

Description	Symbol	Min.	Nom.	Max.	Unit
Logic Supply Voltage	V_{CC}	4.5	5.0	5.5	V
LED Supply Voltage, Display ON [1]	V_{LED}	4.5	5.0	5.25	V
LED Supply Voltage, Display OFF [2]	V_{LED}	–0.5	0	1.0	V
Operating Temperature, Ambient	T_A	–20	25	70	°C

[1] All selected LEDs remain uniformly lit. [2] All LEDs remain off.

Electrical / Optical Characteristics (T_A = –20°C to 70°C, Unless Noted)

Description	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Logic Voltage, "0" State	$V_{in\ (0)}$	V_{CC} = 4.5V	0		0.8	V
Logic Voltage, "1" State	$V_{in\ (1)}$	V_{CC} = 5.5V	2.0		5.25	V
Logic Supply Current	I_{CC}	V_{CC} = 5.5V		37 [1]	65	mA
LED Supply Current	I_{LED}	V_{CC} = 5.5V, V_{LED} = 5.25V		250 [1]	460	mA
Power Dissipation	P_D	V_{CC} = 5.5V, V_{LED} = 5.25V		1.4 [1]	2.8	W
Luminous Intensity per LED (digit average)	I	V_{CC} = 5.0V, V_{LED} = 5.0V T_A = 25°C	0.8	1.25		mcd
Logic Current, "0" State	$I_{in\ (0)}$	V_{CC} = 5.5V, V_{in} = 0.4V			–1.6	mA
Logic Current, "1" State	$I_{in\ (1)}$	V_{CC} = 5.5V, V_{in} = 2.4V			+100	μA
Decimal Point Current	I_{dp}	V_{CC} =5.5V, V_{LED} = 5.25V V_{dp} = 0.4V		–25 [2]	–35	mA
Peak Wavelength	λ_{peak}	T_C = 25°C		655		nm
Spectral Halfwidth	$\Delta\lambda_{1/2}$	T_C = 25°C		30		nm
Weight				25		gm

[1] V_{CC}= 5.0V, V_{LED}= 5.0V with statistical average number of LEDs lit, T_A= 25°C.

[2] V_{CC}= 5.0V, V_{LED}= 5.0V, T_A= 25°C.

Truth Table

Character	X8	X4	X2	X1	
0	L	L	L	L	
1	L	L	L	H	
2	L	L	H	L	
3	L	L	H	H	
4	L	H	L	L	
5	L	H	L	H	
6	L	H	H	L	
7	L	H	H	H	
8	H	L	L	L	
9	H	L	L	H	
BLANK	H	L	H	L	
BLANK	H	L	H	H	
BLANK	H	H	L	L	
BLANK	H	H	L	H	
BLANK	H	H	H	L	
BLANK	H	H	H	H	
D.P. ON		D.P. (IN) = L			
D.P. OFF		D.P. (IN) = H			

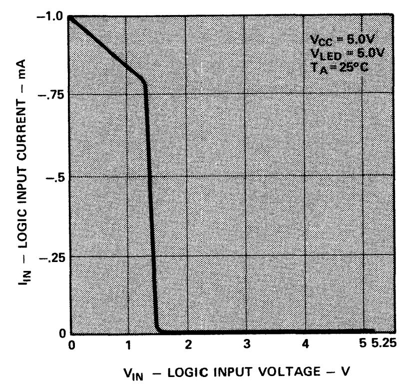


Figure 1. Typical BCD logic input current vs. input voltage.

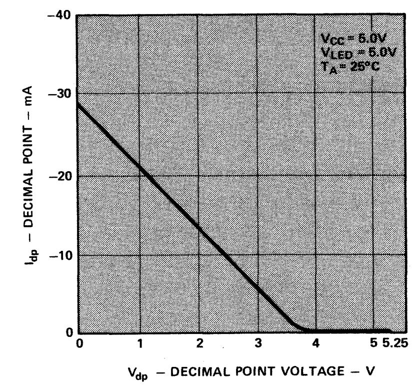


Figure 2. Typical decimal point input current as a function of dp input voltage.

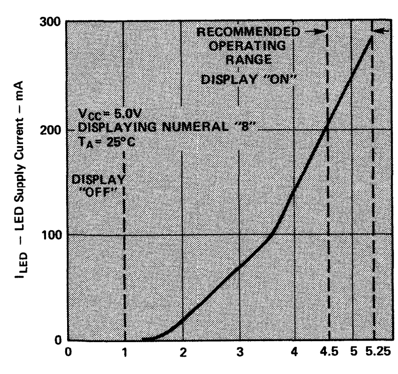


Figure 3. Typical I_{LED} as a function of V_{LED}.

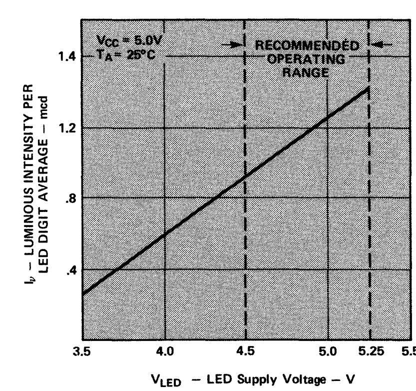


Figure 4. Typical luminous intensity per LED (digit average) as a function of V_{LED}.

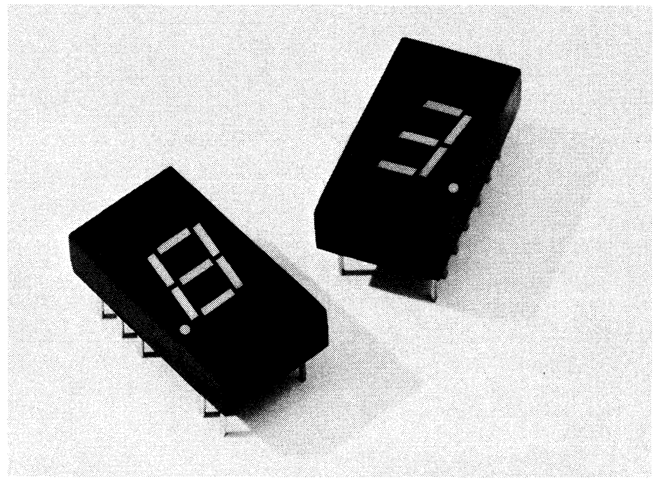
HEWLETT hp PACKARD
COMPONENTS

0.3" SOLID STATE SEVEN SEGMENT INDICATOR

5082-7730 SERIES

Features

- 5082-7730
  - Common Anode
  - Left Hand D.P.
- 5082-7731
  - Common Anode
  - Right Hand D.P.
- Excellent Character Appearance
  - Continuous Uniform Segments
  - Wide Viewing Angle
  - High Contrast
- IC Compatible
  - 1.6V dc per Segment
- Standard 0.3" DIP Lead Configuration
  - PC Board or Standard Socket Mountable
- Categorized for Luminous Intensity
  - Assures Uniformity of Light Output from Unit to Unit within a Single Category



Description

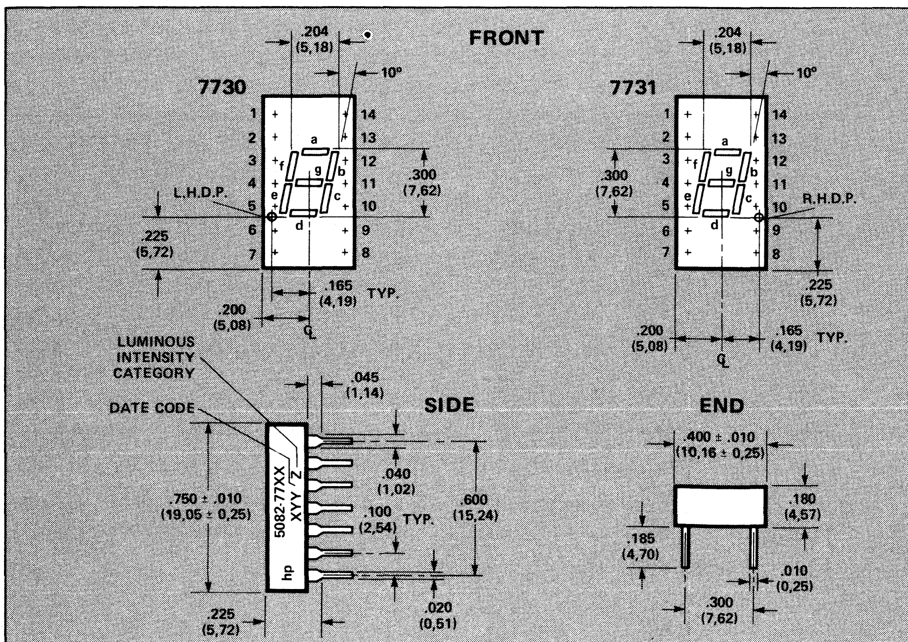
The HP 5082-7730 Series are single digit 0.3" high seven segment indicators. The units employ a new optical magnification technique which converts 8 discrete LED chips into 7 large uniformly intense bars plus a decimal point. The use of a standard DIP package allows for socket and PC board mounting. These techniques combine to offer low cost, improved character appearance, and increased reliability.

The 5082-7730 is a common anode seven segment indicator which employs a left-hand decimal point. Typical applications include electronic instrumentation, computer systems, and business machines.

The 5082-7731 is a common anode seven segment indicator which employs a right hand decimal point. Typical applications include electronic calculators and business terminals such as credit card verifiers.

Low cost and high reliability make these devices ideal for consumer applications such as automobiles, TVs, radios and clocks.

Package Dimensions



PIN	FUNCTION 5082-7730	FUNCTION 5082-7731
1	CATHODE - a	CATHODE - a
2	CATHODE - f	CATHODE - f
3	ANODE[3]	ANODE[3]
4	NO PIN	NO PIN
5	NO PIN	NO PIN
6	CATHODE - dp	NO CONN.[4]
7	CATHODE - e	CATHODE - e
8	CATHODE - d	CATHODE - d
9	NO CONN.[4]	CATHODE - dp
10	CATHODE - c	CATHODE - c
11	CATHODE - g	CATHODE - g
12	NO PIN	NO PIN
13	CATHODE - b	CATHODE - b
14	ANODE[3]	ANODE[3]

NOTES:
1. Dimensions in inches and (millimeters).
2. Tolerances on all dimensions are ± .015" (± 0,38) unless otherwise specified.
3. Redundant anodes.
4. Leave pin unconnected.

Absolute Maximum Ratings

Power Dissipation T_A = 25°C	400 mW
Operating Temperature Range	−20°C to + 85°C
Storage Temperature Range	−20°C to + 85°C
Average Forward Current/Segment or Decimal Pt. T_A = 25°C [1]	25 mA
Peak Forward Current/Segment or Decimal Pt. T_A = 25°C (Pulse Duration ≤ 500 μs)	150 mA
Reverse Voltage/Segment or Decimal Pt.	6V
Max. Solder Temperature 1/16″ Below Seating Plane (t ≤ 5 sec.) [2]	230°C

NOTES: 1. Derate from 25°C at .25 mA/°C per segment or D.P. 2. Clean only in Freon TF, Isopropanol, or water.

Electrical/Optical Characteristics at T_A=25°C

Description	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment [1]	I_ν	I_F = 20 mA	100	250		μcd
Peak Wavelength	λ_{peak}			655		nm
Forward Voltage/Segment or D.P.	V_F	I_F = 20 mA		1.6	2.0	V
Reverse Current/Segment or D.P.	I_R	V_R = 6V			100	μA
Rise and Fall Time [2]		t_r, t_f		10		ns
Temperature Coefficient of Forward Voltage	ΔV_F/°C			−2.0		mV/°C
Temperature Coefficient of Luminous Intensity	ΔI_ν/°C			−1.0		%/°C

NOTES: 1. The digits are categorized for luminous intensity such that the variation from digit to digit within a category is not discernible to the eye. Intensity categories are designated by a letter located on the right hand side of the package.
2. Time for a 10%-90% change of light intensity for step change in current.

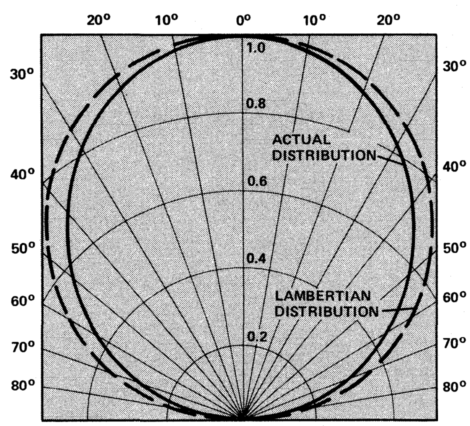


Figure 1. Normalized Angular Distribution of Luminous Intensity.

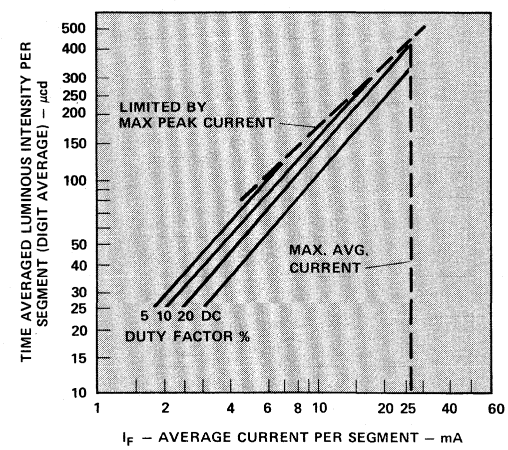


Figure 2. Typical Time Averaged Luminous Intensity per Segment versus Average Current.

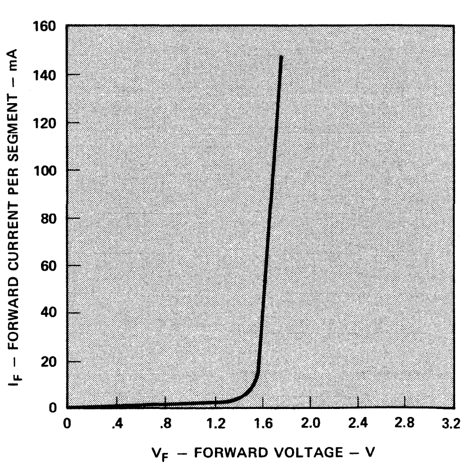


Figure 3. Forward Current versus Forward Voltage.

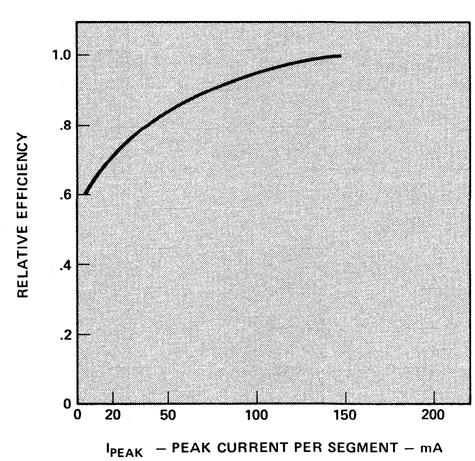


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) versus Peak Current per Segment.

Truth Table

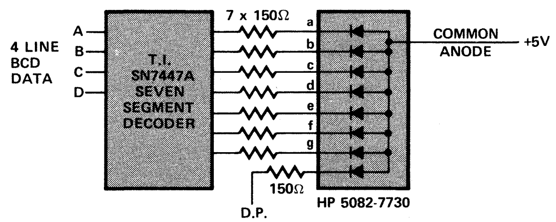


Figure 5. Direct Drive Circuit for the 5082-7730/7731 Common Anode Display.

DECIMAL VALUE	BCD INPUTS				5082-7730/7731 SEGMENT OUTPUTS							FONT
	D	C	B	A	a	b	c	d	e	f	g	
0	0	0	0	0	1	1	1	1	1	1	0	
1	0	0	0	1	0	1	1	0	0	0	0	
2	0	0	1	0	1	1	0	1	1	0	1	
3	0	0	1	1	1	1	1	1	0	0	1	
4	0	1	0	0	0	1	1	0	0	1	1	
5	0	1	0	1	1	0	1	1	0	1	1	
6	0	1	1	0	0	0	1	1	1	1	1	
7	0	1	1	1	1	1	1	0	0	0	0	
8	1	0	0	0	1	1	1	1	1	1	1	
9	1	0	0	1	1	1	1	0	0	1	1	
10	1	0	1	0	0	0	0	1	1	0	1	
11	1	0	1	1	0	0	1	1	0	0	1	
12	1	1	0	0	0	0	1	1	1	0	0	
13	1	1	0	1	1	0	0	1	0	1	1	
14	1	1	1	0	0	0	0	1	1	1	1	
15	1	1	1	1	0	0	0	0	0	0	0	

Note: 1 = Segment ON
0 = Segment OFF

Electrical

The common anode 5082-7730/5082-7731 are arrays of eight discrete light emitting diodes, which are optically magnified to form seven individual segments plus a decimal point. Character encoding on either device can be performed by commercially available BCD-7 segment decoder/driver circuits. Through the use of strobing techniques, only one decoder/driver is required to drive a display containing up to 16 characters as outlined in Figure 6 below. When each character in the display is illuminated in sequence, at a minimum of 100 times per second, flicker-free characters are formed. Under average current drive conditions of 10mA/segment, the display is easily readable to distances of ten feet and will retain good contrast under relatively high ambient lighting conditions.

Mechanical

The 5082-7730 and 5082-7731 devices are constructed utilizing a lead frame in a standard DIP package. The individual packages may be close-packed at 400 mil centers on a PC board. Also, the larger character height allows other character spacing options where desired. The lead frame has an integral seating plane which will hold the package approximately .045" above the PC board during standard soldering and flux removal operation. To optimize device performance, new materials are used that are limited to certain solvent materials for flux removal. It is recommended that only Freon TF, Isoproponal, or water be used for cleaning operations. To improve display contrast, the entire front surface of the display, except for the emitting areas, is finished in a uniform flat black. An additional filter, such as Plexiglas 2423 may be incorporated, if desired, to further lower the ambient reflectance and improve display contrast.

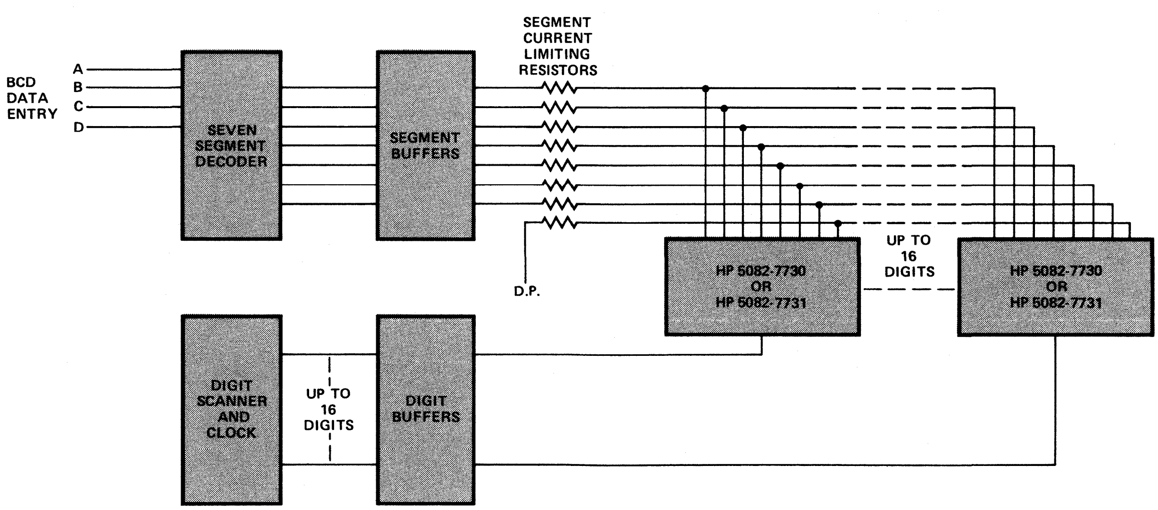


Figure 6. General Strobe Drive Scheme for Common Anode (5082-7730/5082-7731) Displays.

HEWLETT PACKARD

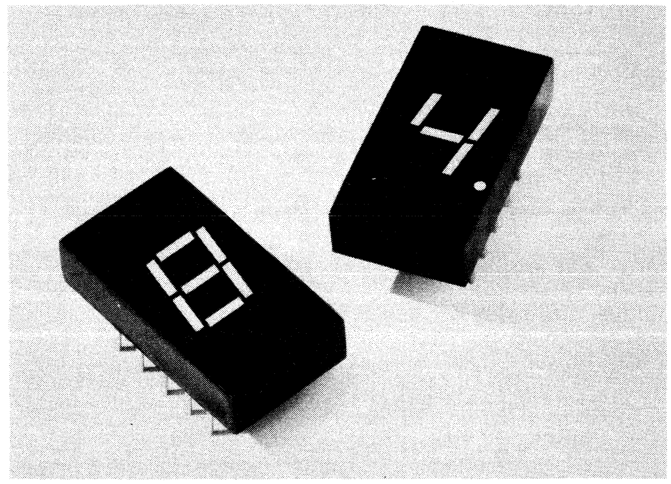
COMPONENTS

0.3" SOLID STATE SEVEN SEGMENT INDICATOR

5082-7740

Features

- COMMON CATHODE
- RIGHT HAND DP
- EXCELLENT CHARACTER APPEARANCE
  - Continuous Uniform Segments
  - Wide Viewing Angle
  - High Contrast
- IC COMPATIBLE
  - 1.7V per Segment
- STANDARD 0.3" DIP LEAD CONFIGURATION
  - PC Board or Standard Socket Mountable
- CATEGORIZED FOR LUMINOUS INTENSITY
  - Assures Uniformity of Light Output from Unit to Unit within a Single Category

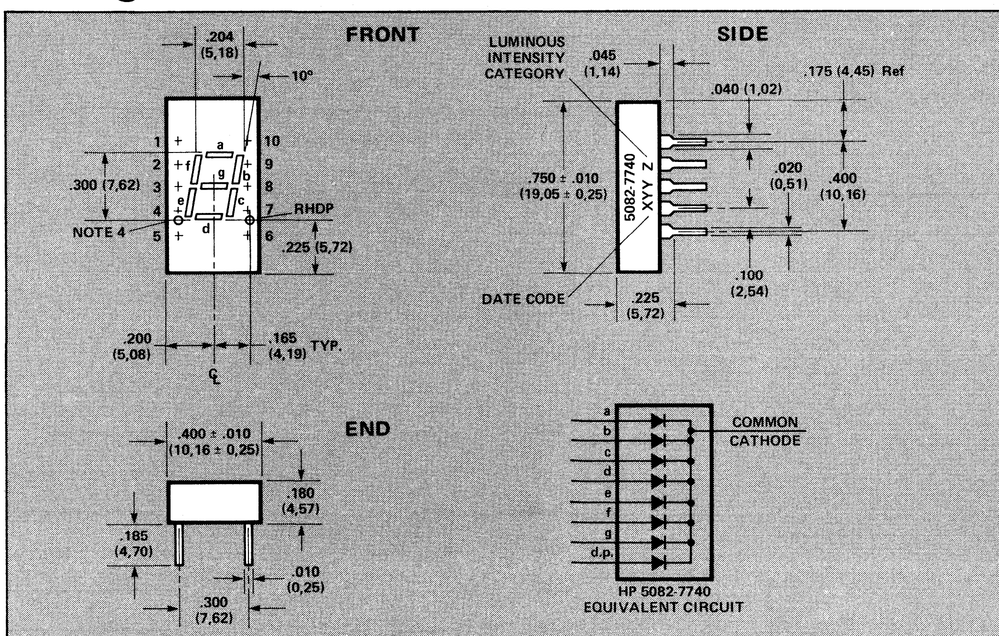


Description

The HP 5082-7740 is a common cathode LED numeric display with a right hand decimal point. The large 0.3" high character size generates a bright, continuously uniform 7 segment display. Designed for viewing distances of up to 10 feet, this single digit display has been human engineered to provide a high contrast ratio and wide viewing angle.

The 5082-7740 utilizes a standard 0.3" dual-in-line package configuration that allows for quick mounting on PC boards or in standard IC sockets. Requiring a forward voltage of only 1.7V, the display is inherently IC compatible allowing for easy integration into electronic calculators, credit card verifiers, TVs, radios, and digital clocks.

Package Dimensions



PIN	FUNCTION 5082-7740
1	CATHODE[3]
2	ANODE - f
3	ANODE - g
4	ANODE - e
5	ANODE - d
6	CATHODE[3]
7	ANODE - dp
8	ANODE - c
9	ANODE - b
10	ANODE - a

NOTES:
1. Dimensions in inches and (millimeters)
2. Tolerances on all dimensions are ± .015" (± 0,38) unless otherwise specified.
3. Redundant cathodes.
4. LHDP not electrically connected.

Absolute Maximum Ratings

Power Dissipation T_A = 25°C	400mW
Operating Temperature Range	−20°C to + 85°C
Storage Temperature Range	−20°C to + 85°C
Average Forward Current/Segment or Decimal Pt. T_A = 25°C [1]	25mA
Peak Forward Current/Segment or Decimal Pt. T_A = 25°C (Pulse Duration ⩽ 500μs)	150mA
Reverse Voltage/Segment or Decimal Pt.	6V
Max. Solder Temperature 1/16" Below Seating Plane (t ⩽ 5 sec.) [2]	230°C

NOTES: 1. Derate from 25°C at .25mA/°C per segment or D.P. 2. Clean only in Freon TF, Isopropanol, or water.

Electrical/Optical Characteristics at T_A=25°C

Description	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment [1]	$I_{\nu\,AVE}$	I_{PEAK} = 100mA 10% Duty Cycle	50	150		μcd
		I_F = 20mA DC		250		
Peak Wavelength	λ_{PEAK}			655		nm
Forward Voltage/Segment or D.P.	V_F	I_F = 100mA		1.6	2.3	V
Reverse Current/Segment or D.P.	I_R	V_R = 6V			100	μA
Rise and Fall Time [2]	t_r, t_f			10		ns
Temperature Coefficient of Forward Voltage	ΔV_F / °C			−2.0		mV/°C
Temperature Coefficient of Luminous Intensity	ΔI_ν/°C			−1.0		%/°C

NOTES: 1. The digits are categorized for luminous intensity such that the variation from digit to digit within a category is not discernible to the eye. Intensity categories are designated by a letter located on the right hand side of the package.
2. Time for a 10%-90% change of light intensity for step change in current.

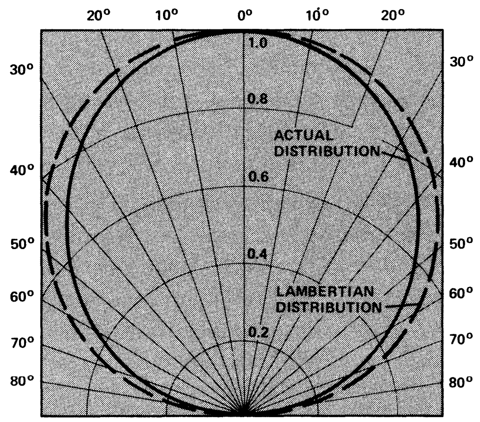


Figure 1. Normalized Angular Distribution of Luminous Intensity.

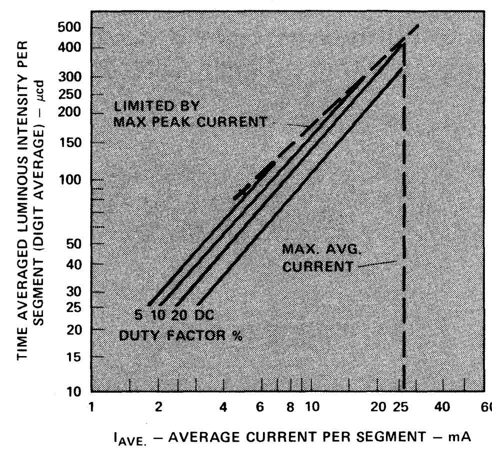


Figure 2. Typical Time Averaged Luminous Intensity per Segment versus Average Current.

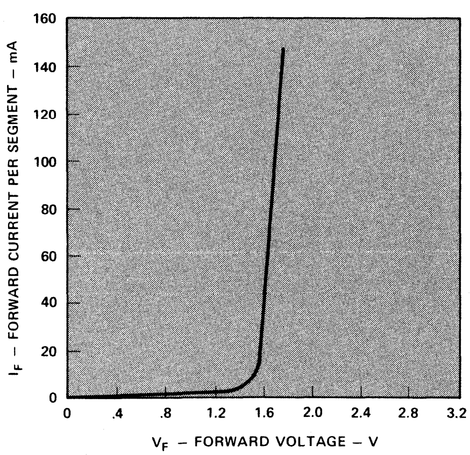


Figure 3. Forward Current versus Forward Voltage.

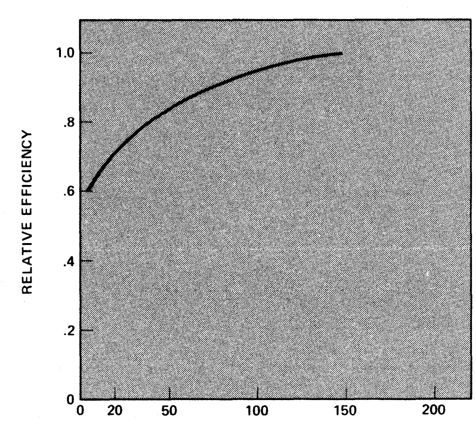
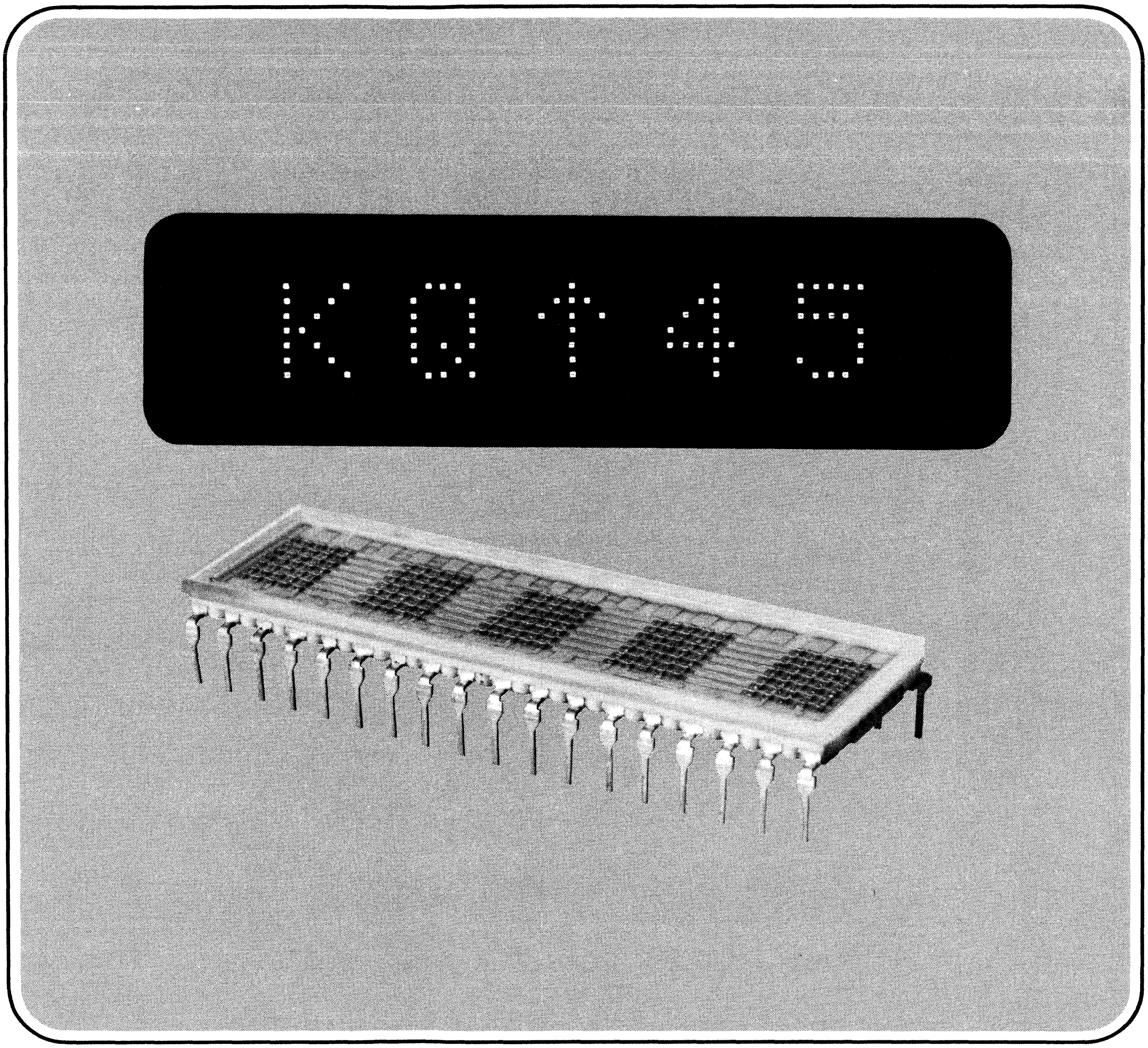


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) versus Peak Current per Segment.

APPLICATION NOTE 931

SOLID STATE ALPHANUMERIC DISPLAY

DECODER/DRIVER CIRCUITRY



HEWLETT hp PACKARD

Introduction

Hewlett Packard offers a series of solid state displays capable of producing multiple alphanumeric characters utilizing 5x7 dot arrays of GaAsP light emitting diodes (LED's). These 5x7 dot arrays exhibit clear, easily read characters. In addition, each array is X-Y addressable to allow for a simple addressing, decoding, and driving scheme between the display module and external logic.

There are three main advantages with the use of the X-Y addressable array:

1. X-Y addressing the 5 column to 7 row, 35 dot array utilizes the minimum number of pin connections.

2. X-Y addressing allows sharing of the read only memory (ROM) character generator and scanning elements over several characters for substantial cost savings.

3. X-Y addressing allows using circuit elements already available in system digital logic circuits such as clock/ timing elements and buffer storage elements.

Methods of addressing, decoding and driving information to such an X-Y addressable matrix are covered in detail in his application note. The note starts with a general definition of the scanning or strobing technique used for this simplified addressing and then proceeds to describe horizontal and vertical strobing. Finally, a detailed circuit description is given for a practical vertical strobing application.

Description of Scanning Techniques

To form alphanumeric characters with an X-Y addressable array of light emitting diodes (LED's), a technique called "scanning" or "strobing" is utilized. This technique is basically timing-sharing of information across the rows or columns of the display, one row or column at a time. Information is addressed to the display by selecting one row (or column) of diodes at a time, energizing the appropriate diodes in that row and then proceeding to the next row. After all rows have been selected, in order, the cycle is repeated. By scanning all rows at least 100 times a second, briefly lighting the appropriate LED's, a flicker-free character composed of illuminated LED's is formed.

When information is scanned from row to row of the display (top to bottom) the mode is called **vertical** strobing. Information can also be scanned from column to column (left to right across the display) in the **horizontal** strobing mode. (See Figure 1.)

Figure 2 indicates how with **vertical** strobing the letters "HP" would be formed by sequentially selecting the rows and energizing the correct diodes in each column. When row I is selected only columns 1A, 1E and 2A, 2B, 2C, 2D

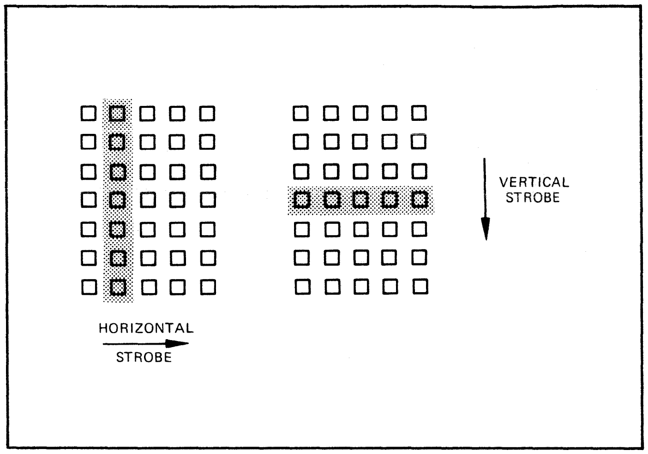


Figure 1.

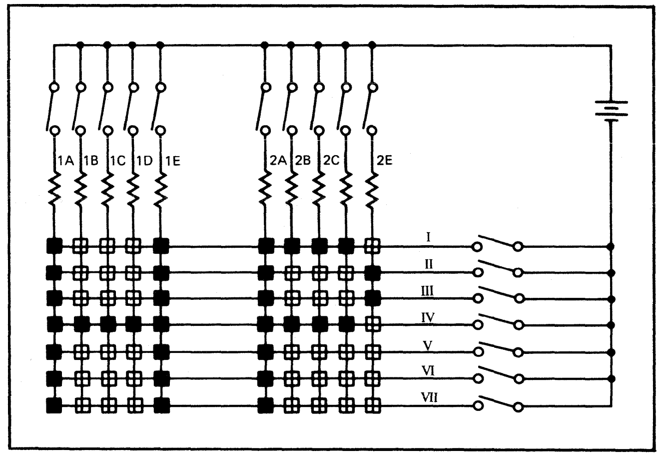


Figure 2.

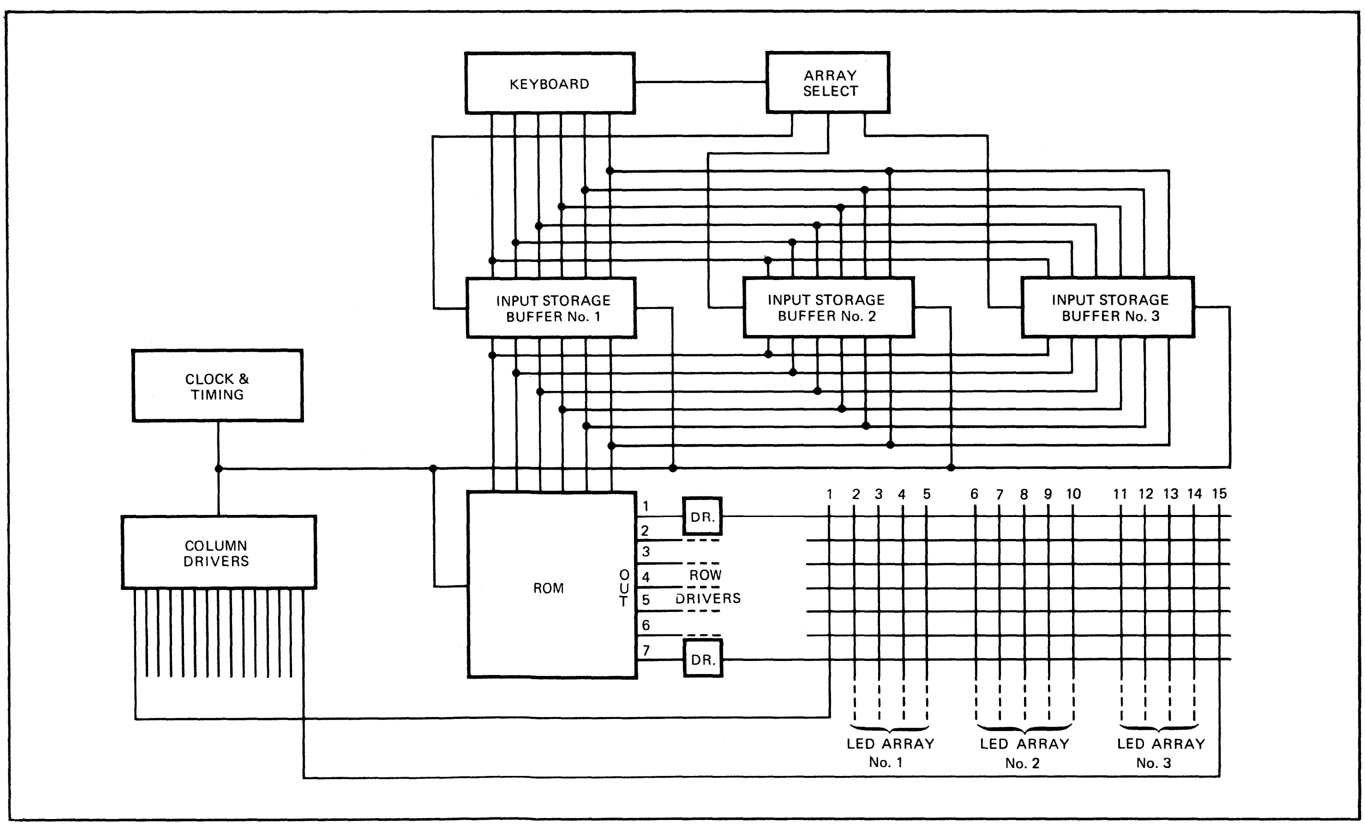


Figure 3. Horizontal Strobing Circuit Block Diagram

are energized. When selecting row II, columns 1A, 1E and 2A, 2E are energized and the process is continued as indicated by the solid squares.

To form the characters "HP" with **horizontal** strobing, the columns would be sequentially selected and the correct diodes in each row lighted. For example, when column 1A is selected, rows I, II, III, IV, V, VI, VII are energized. When selecting column 1B, row IV is energized and the process continues to form "HP", indicated by the solid squares.

Strobing Circuitry

The digital circuitry which performs the high speed sequential switching between rows (or columns) of diodes in strobing, can be classified in four major parts.

1. STORAGE BUFFERS: Flip-flops that store input or output digital information.
2. CLOCK/TIMING CIRCUITRY: A sequential pulse generator that times and keys the activity of all circuit components.
3. READ-ONLY-MEMORY: A character generator that accepts a binary coded input and furnishes a sequential 5x7 dot array information output.
4. ROW AND COLUMN DRIVERS: Current sources necessary to provide proper current drive levels to the LED's.

All of these circuit elements are commercially available in the form of IC's or discrete components.

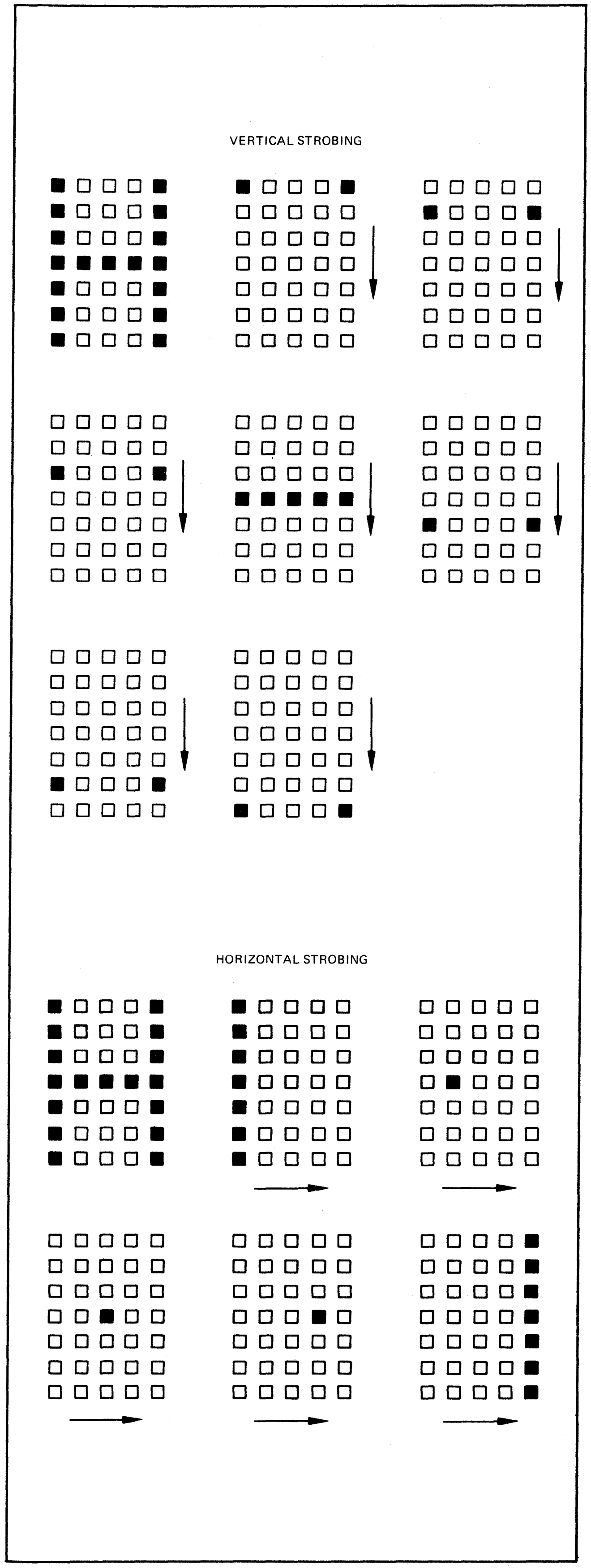
Horizontal Strobing

A simplified circuit diagram for horizontal strobing is shown in Figure 3. This particular technique describes three characters, however, operation of 1 – 4 characters is similar.

A. Coded, 6 bit, alphanumeric information is sequentially entered and stored in three, 6 bit, input storage buffers. The input information code in this example is a 6 bit (line) ASCII, but could be some other code if desired. Information is entered bit parallel, character serial to the appropriate input storage buffer. An array select line steers the information to the proper storage buffer.

B. Next, with the input information stored in the input buffers, timing circuitry enables the ROM and first input storage buffer so its stored 6 bit code is read into the ROM. (All other input storage buffers are disabled.)

C. The 6 bit input is decoded by the ROM and the first column of character information appears at the 7 line output of the ROM. The output signal is converted from a voltage to a current source by the row drivers. At the same time the output signal appears at the appropriate rows, the timing circuitry connects the



Vertical and Horizontal Strobing

first column of the first LED character to complete the current path and light the appropriate diodes.

D. Next, a timing pulse triggers the ROM to present the second column of character information at its 7 line output. Again, the signals are converted to current sources by the output drivers which light the appropriate diodes in the second column with connection of the second column drivers.

E. Repeating this sequence. The ROM cycles through the remaining third, fourth and fifth columns.

F. After tracing out the first character, the timing circuitry next enables input storage buffer #2 and information flows to the ROM which, in turn, sequentiallly presents the output character information to the second LED array.

G. Next the third input storage buffer character is decoded by the ROM and sequentially presented to the third LED array.

H. When this cycle is repeated at the rate of 100 times a second or faster, a flicker-free group of characters is formed.

The display duty cycle for each of the 15 vertical columns is about 6.6% and, therefore, the peak currents going into the diodes must be 15 times their average current. The high peak current demand is the reason for the discrete transistor driver stages on both the horizontal rows and vertical columns; about 75 mA peak in this example.

With horizontal strobing, the number of vertical columns that can be energized in one field of scan is limited by the peak current that any one diode can stand. Since the peak current limit of any one diode is about 100 mA and because the diodes require an average of 5 mA for 100 foot Lamberts, then about 20 columns could be run with the horizontal strobing technique.

Vertical Strobing

For applications requiring more than four characters, it is desirable to use the technique of vertical strobing. This mode is similar to horizontal strobing except that the scanning field moves vertically along the seven horizontal rows.

This vertical strobing technique has the advantage that more arrays may be added without affecting the display "ON" duty cycle of the light-emitting diodes. In general, it is a preferrential mode. A typical system is now described in detail.

Vertical Strobing Circuitry

The circuitry is divided into three main functions:

1. The clock and timing circuits,

2. The information handling storage buffers and read only memory (ROM),

3. The current limiting and driver stages.

1. Clock and Timing

In the block diagram of Figure 4, the control function occurs as follows: Data in ASCII code is entered and stored in a series of input storage buffers. The particular circuit described obtains the information from a keyboard which puts out ASCII code as well as an advance pulse. Only one of the input storage buffers is enabled to receive this code at a time. At the receipt of an advance pulse, the timing circuit enables the next input storage buffer.

Another portion of the timing circuit is concerned with getting the ASCII code from the input storage buffers to the character generating ROM, and in getting the character information into the output storage buffers. In the circuit shown, a binary counter and a 1/10 decoder provide the gating pulses for the storage buffers. If the number of arrays in the display is N_A, the binary counter's reset line is connected for counting to N_A (i.e., a mod N_A counter). The input storage buffer #1 is energized at its output at the same time that the output storage buffer #1 is energized at its input. Likewise, input storage buffer #2 and output storage buffer #2 are always operated together.

The total number of arrays that can be serviced by a single ROM is a function of the minimum field rate and line duty cycle, the ROM's access time (approximately 1 microsecond) and how fast the output storage buffers can be loaded (approximately 50 nanoseconds). With a field rate of 140 Hz and a 90% row duty cycle, up to 100 arrays could be serviced by one ROM. The field rate is well above the flicker rate that is visible to the eye. However, each application should consider if the display is subject to vibration during operation. Since the LED's are so fast in switching speed, – and have no persistance after the drive current is turned off, the eye will notice some character breakup if there is vibration of the display. This can be alleviated by speeding up the clock and corresponding field rate.

For a very large number of arrays, or a multi-line matrix of arrays, there may be better ways of partitioning the scan. For example, the ROM might be shared among different clusters of arrays with some additional switching. These circuits are intended primarily as examples and the particular application should determine how a given timing circuit or data handling circuit is designed.

2. Storage Buffers and ROM

The input storage function is one of the most flexible portions of the design. Information may come in a number of forms, including character serial or parallel ASCII code to each input buffer. The basic function however, is to present and store six or seven bit ASCII code in a series of input buffers.

The input storage buffers, as shown in the diagram, all have parallel outputs to the ROM. Thus, whenever the code in a given input buffer is gated out by a pulse from the timing circuitry, the buffer's ASCII information will be presented to the ROM's input.

In theory, the ROM could be used to decode all 35 bits of an ASCII coded character and store them in a read-write memory. However, the 35 bits per array would be relatively expensive so modified and less expensive approach is shown.

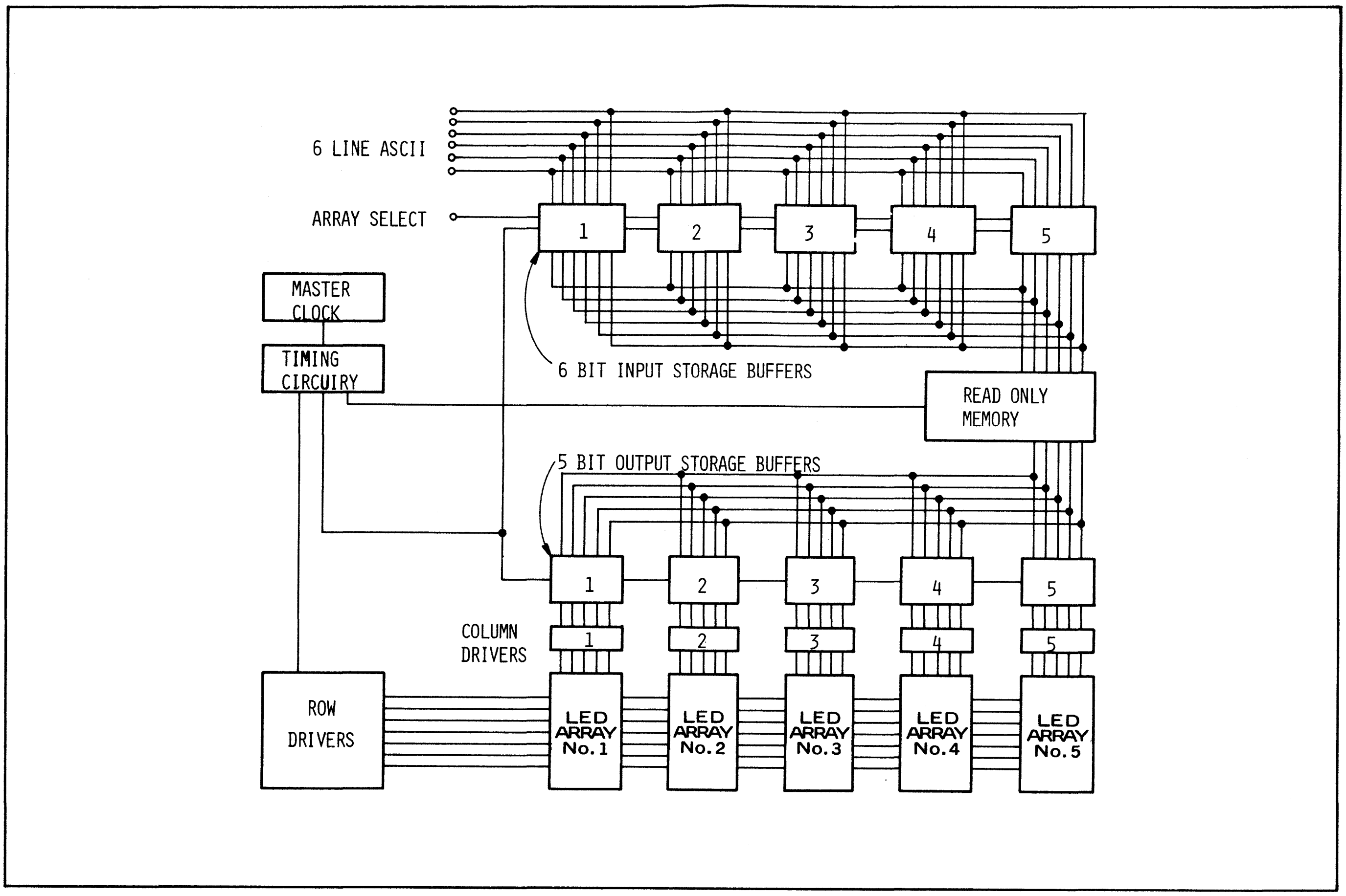


Figure 4. Vertical Strobing - Block Diagram

Assume that we are writing horizontal row number I, for all of the LED arrays. This means that for LED array #1, we need five bits stored in its output storage buffer which represent the five diodes in the top row of the character to be presented. The input storage buffer for LED array #1 is energized and applies its ASCII code to the ROM's input while the ROM is triggered to provide a five line output which represents the five bits of the top row of the character. Output storage buffer #1, corresponding to LED array #1, is then enabled to receive and store this five bit word. Next, ASCII information in input storage buffer #2 is fed to the ROM and a resulting five bit top row word is fed and enabled into output storage buffer #2. This sequence is continued for as many input storage buffers and output storage buffers as there are characters to be displayed.

3. Current Limiting and Driver Stages

After the output storage buffers are loaded with column drive information, the appropriate horizontal row is turned on to complete the current path. In this case, with the top row, row number I, the timing circuitry switches on the row I driver. This allows any light-emitting diode along the entire top row of the display to be energized wherever there is a vertical column driver turned on. Thus, if all the characters to be displayed were "T", the top row driver would enable all of those light-emitting diodes. At the same time, each of the output storage buffers would show that all five diodes on top of each array should be lit, and therefore, all five columns would be energized in every array.

Ignoring the relatively small load time, in vertical strobing the display cycle for seven line characters is 1/7 or approximately 14% of the total time on. In general, it is recommended that the strobing take place at as high a field rate as feasible. In this case, the circuitry shown represents a field rate of 125 Hz. Thus, the on-time for each row is 1150 microseconds, assuming the load time is negligible. After row number I is energized for one 1/7 of the total duty cycle, the timing circuitry directs the ROM to read the input storage buffers and to load the output storage buffers with the bits required to display row number II for each character. At that point, row number II is switched **on** by the row driver transistor which stays on for one 1/7 of the total duty cycle.

Because of duty cycle considerations, the diodes must be driven at relatively high peak currents, since they will only be on for one 1/7 of the time. For the vertical column drivers, the diode must be driven with a current that is seven times the average current so that the eye will average the light output. Assuming that an average current of five mA is adequate for approximately 100 fL light output, then the column drivers must handle 35 mA peak current. The drive circuitry, as shown in Figure 5 is arranged so that

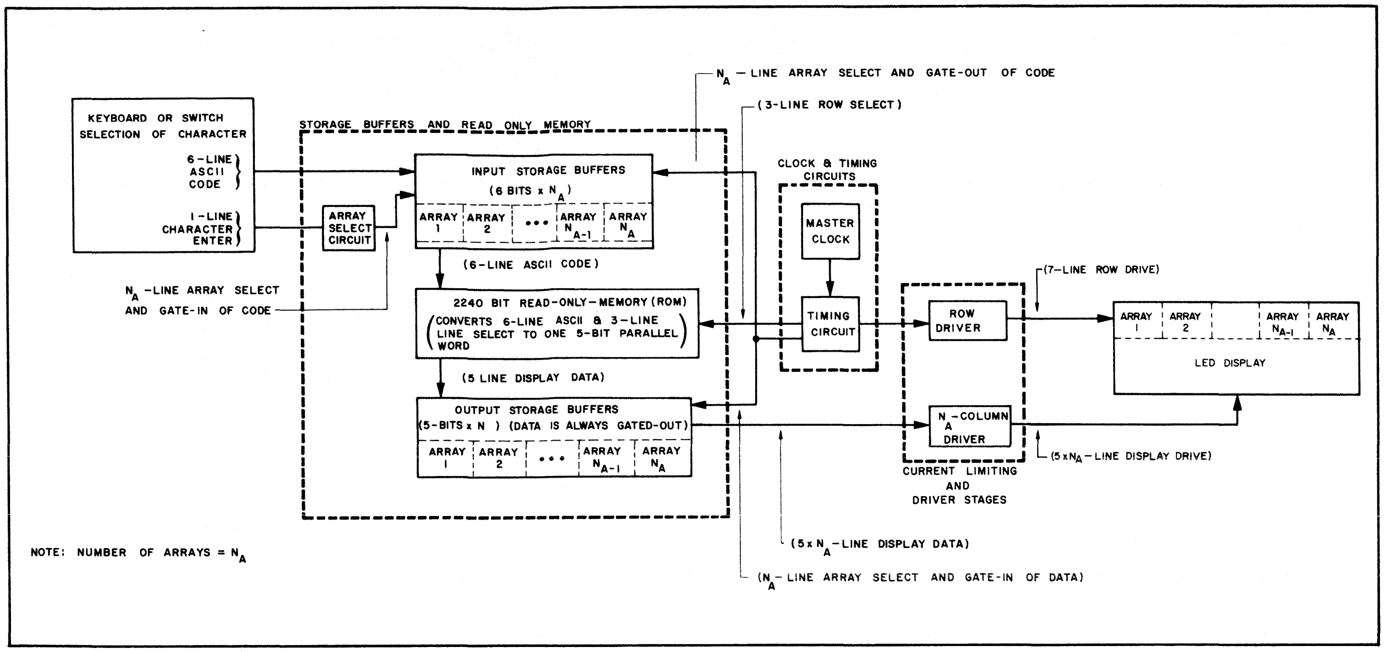


Figure 5. Vertical Strobing - Detailed Block Diagram

limiting is provided by the column driver stages. Two different methods of column drive are possible. Discrete transistors with the peak capabilities required are readily available and inexpensive. They generally cost less than 25¢ in large quantities. Also, a number of power gates (e.g., Motorola MC858) and multiple core drivers (e.g. Fairchild SH6502) will handle these currents.

Since the current limiting takes place primarily at series resistor in the vertical column drive, the large switch transistor which is used to enable the horizontal row only has to be an on-off type of switch. It would be impossible to current limit on the horizontal row because the circuit would not know how many diodes were to be turned on. The peak row current can be high, since it must switch drive currents to all the light-emitting diodes along its line. As an example, if the characters being displayed are "T"'s and there are 10 characters, then 50 diodes must be enabled. With a peak current of 35 mA for each diode and 50 diodes, over 1.7 amps switching current is needed. The row driver transistors, as noted on the materials list, are adequate for up through 10 arrays. If more arrays are needed, one can either use higher rated row drivers or divide the display into groups of arrays with each group having its own row driver stage. A buffer stage following the 9301 1/10 decoder may be needed to drive the additional loads.

Since LED efficiency increases with operating current, additional display efficiency is gained through strobing. It should also be noted that it's easy to adjust the display's intensity by changing the row duty cycle of the row drivers. The application is set up so that the on-time of the horizontal row switches can be varied. Thus, if the on-time for ach horizontal row were cut from 1150 microseconds to 575 microseconds, while the field rate is constant, intensity would be halved. This function is not shown on the circuit diagram.

System Interface

The area with greatest potential cost savings is the timing and drive circuitry. In the display circuitry shown, the timing is set up with commercially available circuits. In many applications, a substantial amount of timing and shift register clock phases may already be available and can be used as part of the strobing circuitry. As an example, if the character code is stored in existing shift registers, then a separate input storage buffer may not be needed. Instead, a set of character serial, bit parallel ASCII lines could be fed directly into the ROM with its own time sequence.

Pin Requirements

In the 5x7 dot array, each of the light-emitting diodes is mounted at the intersection of an X and a Y drive line. The display therefore acts much like a cathode ray tube with the X-Y input address determining which diode or set of diodes lights. Each array is a 5x7 matrix requiring five vertical column drive lines and seven horizontal row drive lines. Drive line economy is achieved by clustering arrays since all of the horizontal rows run in parallel. Thus, the total number of pin connections of such a package is 7 (for horizontal drive rows) plus $5N_A$ (for vertical drive columns), where N_A is the number of arrays in the display package. Within any package, the current per line should never exceed 2 amps.

Circuit Changes to Vertically Strobe Other Than 5 Arrays

The vertical strobing circuitry described previously was specifically designed for flexibility in strobing between four and ten arrays. For each additional array above five, the following components are needed:

3 SN7475N Quad Latch DIP's;

5, 33 ohm, 5%, 1/4 W resistors;

2, 2 K ohm, 5%, 1/4 W resistors;

1/4, MC3003P Quad 2-input OR Gate DIP;

1 3/4, MC858P Quad 2-input Power NAND Gate DIP's;

1 1/2, 9946 Quad 2-input NAND Gate DIP's.

Similarly, the drive circuitry for a four array display requires less components than for five arrays by the amount listed above. Actual component and wiring changes are described below:

A. Master Clock and Timing Circuits

1. 1/10 decoder that drives IG2- and ϕG-:
   For each additional array, one more output line of the decoder is utilized, requiring one more 2-input Power NAND Gate (1/4 – MC858P) and one more 2K ohm pull-up resistor. Connection of the additional NAND Gate is similar to those already present.

B. Storage Buffers and Read-Only-Memory

1. **Input Storage Buffers:**
   Since for each additional array one more 6-line ASCII coded character needs to be stored, 1 1/2 – SN7475N Quad Latch DIP's for output gating. Connection of gating lines is the same as for the other input storage buffers.

2. **Output Storage Buffers**
   As with the input storage buffers, for each additional array, 1 1/2 – SN7475N Quad Latch DIP's are needed for the output storage buffer. Gating connections follw those used in the other output storage buffers.

3. **Array Select Circuit:**
   Changes here are similar to those made for the 1/10 decoder in the clock and timing circuits block. For each additional array, one more output line of the decoder is utilized, along with another 2-input power NAND Gate (1/4 – MC858P) and 2 K ohm pull-up resistor, and another 2-input OR Gate (1/4 – MC3003P). The reset signal is taken from the N_A output line (except for $N_A = 10$, where the "9" line is used).

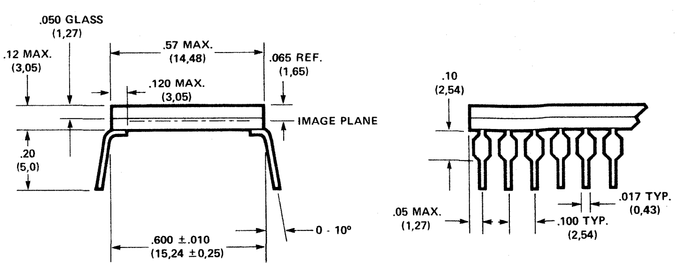
C. Current Limiting and Driver Stages

1. **Column Drivers**
   For every added array, five more 33 ohm resistors and 2-input Power NAND Gates (1 1/4 – MC858P) are required.

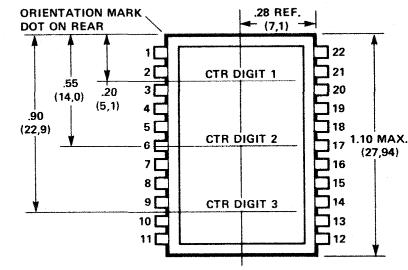
2. **Row Drivers**
   The drive current is a function of N_A ($I_C = (5)$ (35 mA) (N_A)). The values of resistors R_1 and R_2 are dependent on this current, and therefore, on the number of arrays. However, the variance of optimum values is so small that the resistors can be kept the same for displays of between four and ten arrays.

Package Dimensions and Pin Configurations

5082-7100/7101/7102

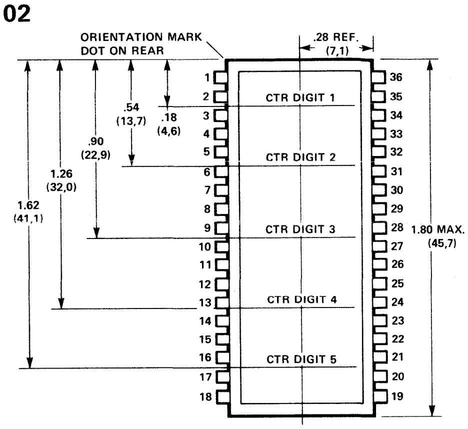


5082-7100



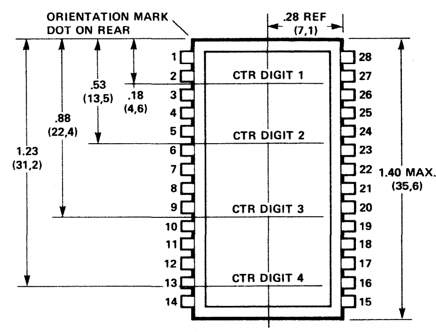
PIN NO.			PIN NO.		
1.	VII	(+)	12.	II	(+)
2.	1C		13.	3D	
3.	1D		14.	3B	
4.	VI	(+)	15.	I	(+)
5.	V	(+)	16.	2E	
6.	2B		17.	2C	
7.	2D		18.	2A	
8.	III	(+)	19.	IV	(+)
9.	3A		20.	1E	
10.	3C		21.	1B	
11.	3E		22.	1A	

5082-7102



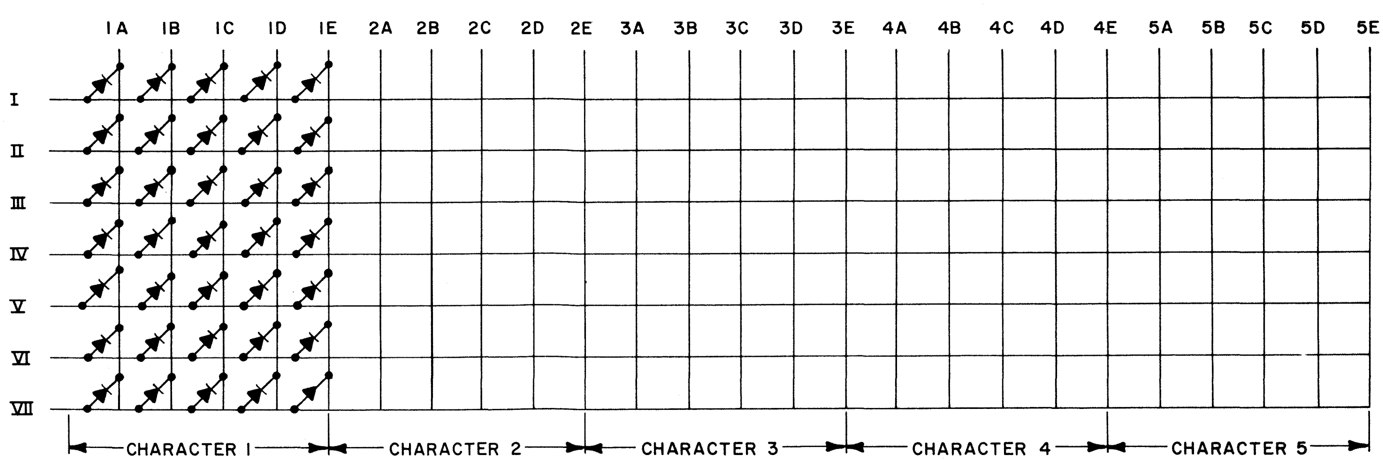
PIN NO.			PIN NO.		
1.	OPEN		19.	5E	
2.	1C		20.	5C	
3.	1E		21.	5A	
4.	VI	(+)	22.	IV	(+)
5.	2B		23.	4E	
6.	2D		24.	4C	
7.	2E		25.	OPEN	
8.	V	(+)	26.	III	(+)
9.	3C		27.	3D	
10.	3E		28.	3B	
11.	VII	(+)	29.	3A	
12.	4A		30.	II	(+)
13.	4B		31.	2C	
14.	4D		32.	2A	
15.	OPEN		33.	I	(+)
16.	5B		34.	1D	
17.	5D		35.	1B	
18.	OPEN		36.	1A	

5082-7101



PIN NO.			PIN NO.		
1.	OPEN		15.	III	(+)
2.	1C		16.	4C	
3.	1E		17.	4A	
4.	VII	(+)	18.	II	(+)
5.	2B		19.	3E	
6.	2D		20.	3B	
7.	IV	(+)	21.	3A	
8.	V	(+)	22.	2E	
9.	3C		23.	2C	
10.	3D		24.	2A	
11.	VI	(+)	25.	I	(+)
12.	4B		26.	1D	
13.	4D		27.	1B	
14.	4E		28.	1A	

NOTES:
1. Dimensions are in inches and (millimeters).
2. Unless otherwise specified, the tolerance on all dimensions is ± .015 inches (± 0,38 mm).
3. Character size .27 x .19 inches (6, 9 x 4, 9 mm).



5082-7100/7101/7102 SCHEMATIC WIRING DIAGRAM

GLOSSARY

1. **ARRAY**: A 5x7 matrix of LED's from which the characters are formed by selective illumination.

2. **ASCII CODE**: A Standard binary code used to represent common symbols and alphanumeric characters. The 6-line version is obtained by dropping the most significant bit from 7-line ASCII. (American Standard Code for Information Interface.)

3. **CHARACTER**: The information or font that is perceived by the observer.

4. **COLUMN**: The vertical string of LED's in an array.

5. **DISPLAY DUTY CYCLE**: Of the time that it takes to cycle through all rows (columns), the percent that one row (column) driver is enabled. In vertical strobing, the Display Duty Cycle = (1/7) (Row Duty Cycle).

6. **FIELD RATE**: The refresh rate of the whole display.

7. **HORIZONTAL STROBING**: A display technique where the information to be displayed is addressed to the arrays by selecting one column of diodes at a time, energizing the appropriate diodes in that column and then proceeding to the next column. After all columns have been selected one at a time, the process is repeated.

8. **LED**: Light Emitting Diode; a diode that emits visible light.

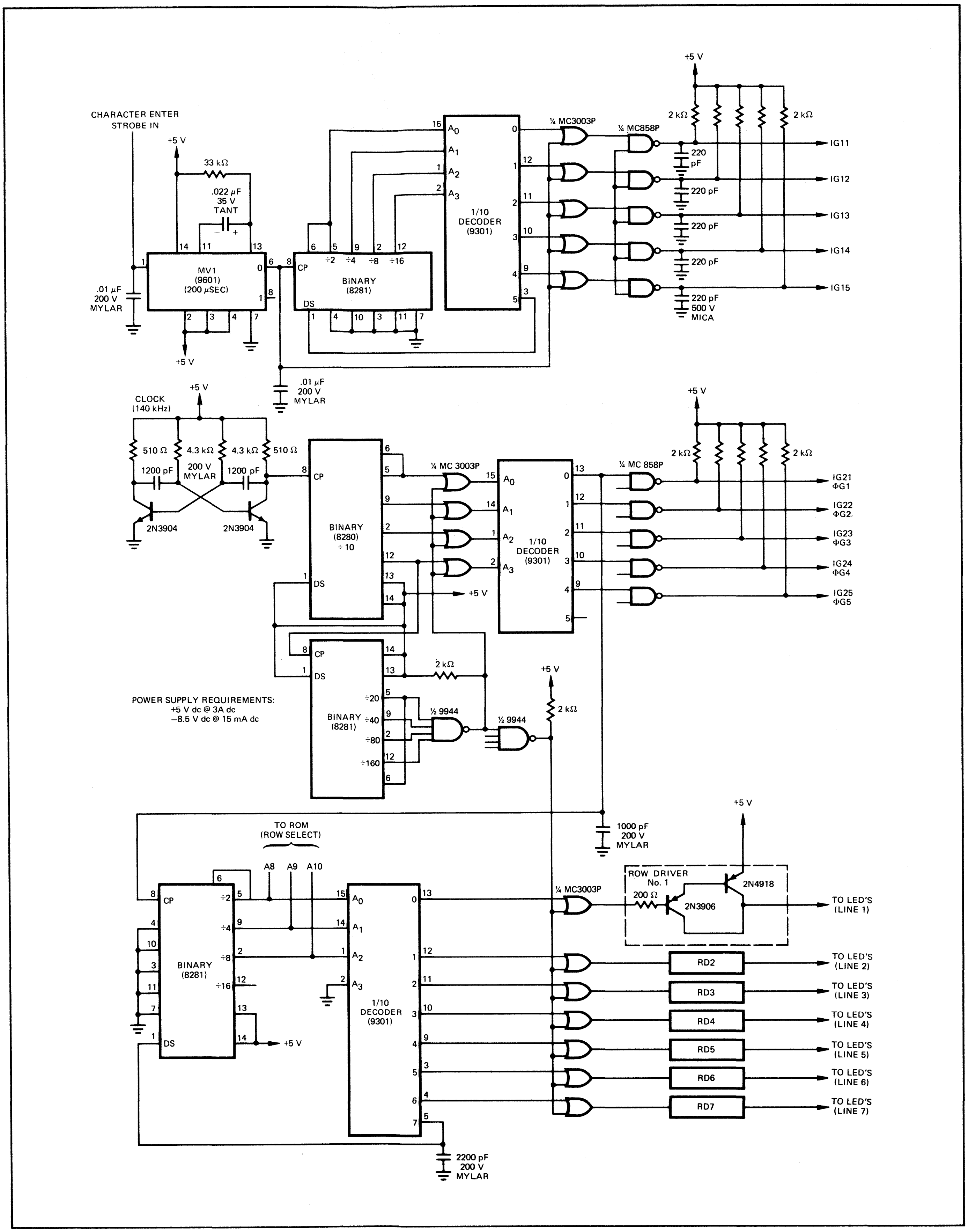
9. **N_A**: The number of arrays in a display.

10. **ROM**: Read Only Memory; an electronic "reference table" of fixed information, where the input determines what data we "look up". The ROM used here provides the 5x7 (35 points) character font data for any one of 64 different alphanumeric characters and symbols. (2240 bits.)

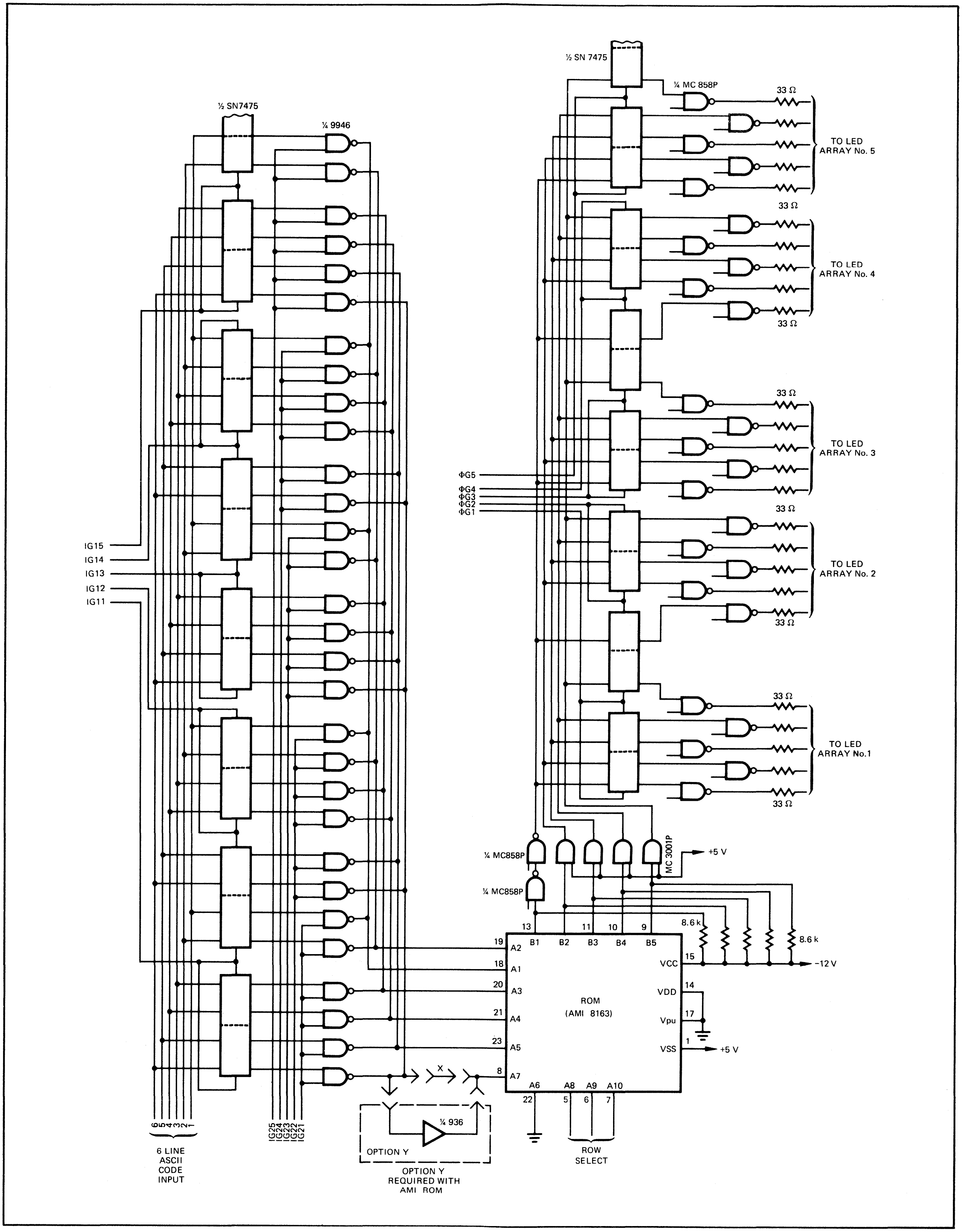
11. **ROW**: The horizontal string of LED's in an array.

12. **ROW DISPLAY DUTY CYCLE**: Of the total time spent loading and displaying a row of information in vertical strobing, the percent (of time) that we display the information.

13. **VERTICAL STROBING**: A display technique where the information to be displayed is addressed to the arrays by selecting one row of all arrays at a time, energizing the appropriate diodes in that row and then proceeding to the next row. After all seven rows have been elected one at a time, the process is repeated.



P/O 5 Character Vertical Strobing Schematic Diagram



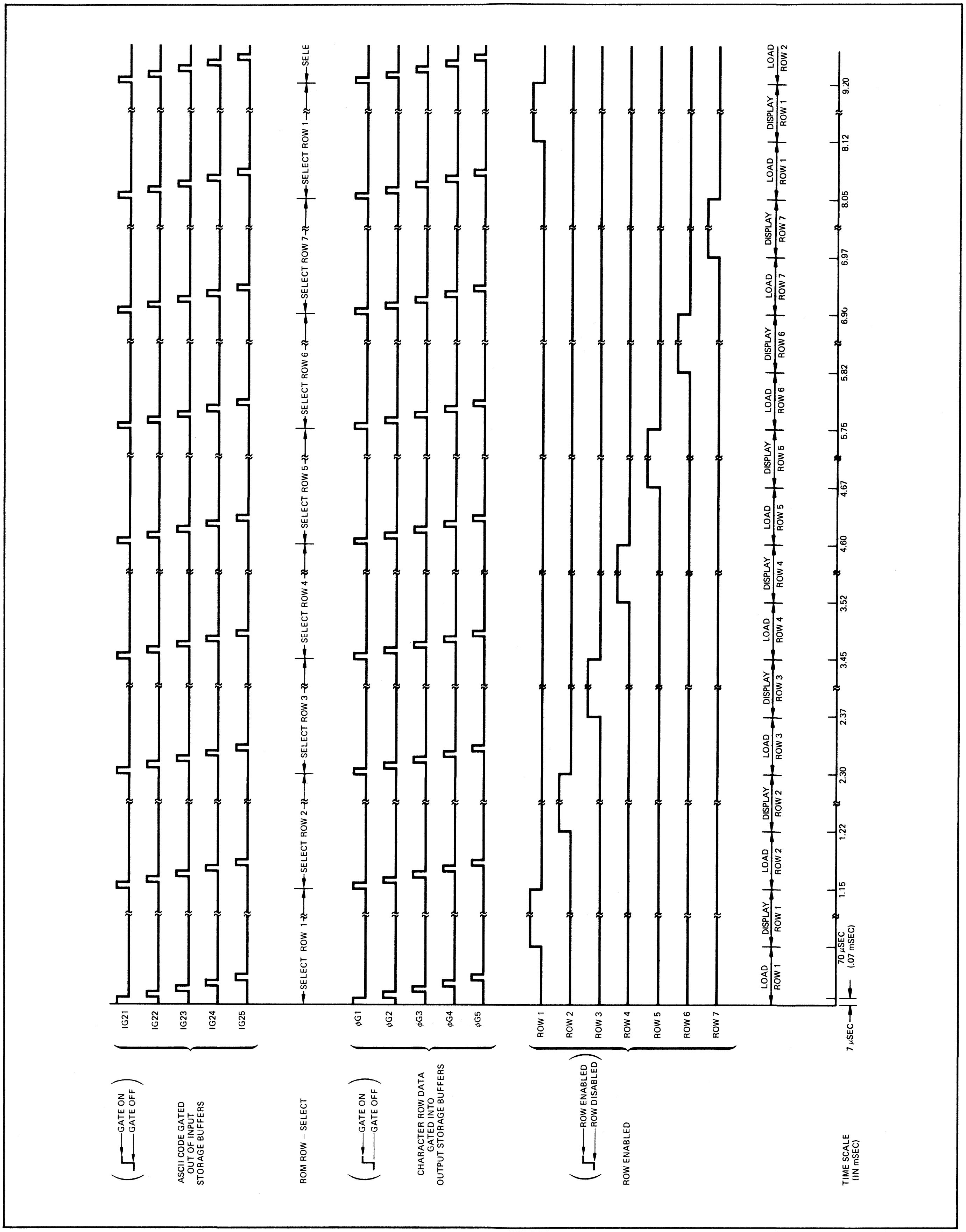
P/O 5 Character Vertical Strobing Schematic Diagram

5 ARRAY VERTICAL STROBED DRIVE CIRCUIT – PARTS LIST

Item (Mfg.)	Description	Quantity
8280 (Signetics)	4-Bit Decade Counter	1
8281 (Signetics)	4-Bit Binary Counter	3
9301 (Fairchild)	T^2L 1/10 Decoder	3
9946 (Fairchild)	DTL Quad 2-input NAND Gates	8
MC858P (Motorola)	DTL Quad 2-input Power NAND Gates	10
MC3003P (Motorola)	T^2L Quad 2-input OR Gates	4
SN7475N (Motorola)	T^2L Quad Latch	16
9601 (Fairchild)	Monostable Multivibrator	1
S8163 (AMI) *	2240-Bit ROM with 5 line output	1
MC3001P (Motorola)	T^2L Quad 2-input AND Gates	1
9944 (Fairchild)	DTL Dual 4-input Power NAND Gates	1
2N3904 (Motorola)	NPN Si Transistor	2
2N3906 (Motorola)	PNP Si Transistor	7
2N4918 (Motorola)	PNP Medium Power Transistor	7
36 pin DIP socket (Cambion)	Socket #703-3791-01-04-16	1
Capacitor	220 pF, 500 V, mica	5
Capacitor	1000 pF, 200 V, mylar	1
Capacitor	1200 pF, 200 V, mylar	2
Capacitor	2200 pF, 220 V, mylar	1
Capacitor	0.022 μF, 35 V, tantalum	1
Capacitor	0.01 μF, 200 V, mylar	2
Capacitor	150 μF, 15 V, tantalum	3
Resistor	33 Ω, 5%, C, 1/4 W	25
Resistor	200 Ω, 5%, C, 1/4 W	7
Resistor	510 Ω, 5%, C, 1/4 W	2
Resistor	2 kΩ, 5%, C, 1/4 W	12
Resistor	4.3 kΩ, 5%, C, 1/4 W	2
Resistor	8.6 kΩ, 5%, C, 1/4 W	5
Resistor	33 kΩ, 5%, C, 1/4 W	1

* The following list illustrates additional 2240 bit character generators which are suitable for vertically strobing 5 x 7 alphanumeric displays. However, since these ROM's are not necessarily PIN replaceable with the AMI S8163 and may require a V_{SS} of greater than 5 v and 2 phase clocks, some minor redesign will be necessary to make the units compatible with the circuit illustrated on pages 10 and 11.

Manufacturer	Part Number
Electronic Arrays	EA 3501
Fairchild	3257
Central Instruments	RO-1-22-40
Mostek	MK2100P
National	5240
Texas Instruments	2400

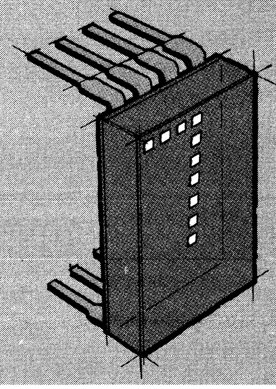


5 Character Vertical Strobing Timing Diagram

HEWLETT PACKARD

COMPONENTS

APPLICATION NOTE 934



5082-7300 Series Solid State Display Installation Techniques

INTRODUCTION

The 5082-7300 series Numeric/Hexadecimal Indicators are an excellent solution to most standard display problems in commercial, industrial and military applications. The unit integrates the display character and associated drive electronics in a single package. This advantage allows for space, pin and labor cost reductions, at the same time improving overall reliability.

The information presented herein describes general methods of incorporating the -7300 into varied applications.

DISPLAY MOUNTING

The 5082-7300 series display modules are designed to be plugged into a DIP connector, or soldered to a PC board. Each display has 8 leads in a dual-in-line configuration. The lead-to-lead spacing is .100" and the horizontal spacing between lines is .600".

Displays can be end-stacked with .100" spacing between outside pins of adjacent units. This allows the use of the many DIP connectors, designed for MSI - LSI integrated circuits, to mount a cluster of display modules. For example, a 40-pin .600" socket can be used to mount 5 display modules. Table I lists several commercially available connectors which can be used to mount the -7300 series displays.

The Jermyn series is recommended for applications where the device is to be heat sinked (see following section for heat sinking requirements), and when it is desired to end stack connectors. These connectors, however, should be soldered into a PC board or used in a similar pin restraining application. Multiple insertions into these connectors tends to push the connecting clip out of the plastic housing. 8N connector pins are required for N digits in a cluster.

Manufacturer	Part Number	Number of Pins	Notes
Jermyn	A23-2023Z	24	Solderable
Jermyn	A23-2031Z	28	Solderable
Jermyn	A23-2025Z	36	Solderable
Jermyn	A23-2030Z	40	Solderable
Cambion	703-3790-01-04-16	24	Solderable
Cambion	703-3896-01-01-16	24	Wire Wrap
Cambion	703-3791-01-04-16	36	Solderable
Cambion	703-3893-01-03-16	36	Wire Wrap
Augut	324-AG2D	24	Wire Wrap
Augut	336-AD2D	36	Solderable
Robinson-Nugent	IC-246	24	Solderable
Robinson-Nugent	IC-366	36	Solderable

Table I

The Jermyn connectors can be end-stacked with a typical .050" additional pin-to-pin interstitial space. Figure 1 shows a typical mounting configuration using these connectors:

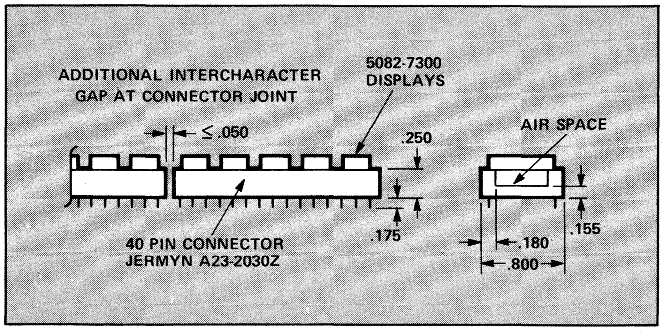


Figure 1. Typical Connector Mounted Array of Display Modules

The Jermyn connectors also provide a space between the back of the display module and the plastic connector housing. When left unfilled, this space allows for air circulation to improve heat transfer by convection and radiation. Heat sinking material can also be placed in this gap.

PC BOARD MOUNTING

The 5082-7300 series can be soldered into a PC board at a maximum solder temperature of 230°C for 5 seconds. The DIP leads on the display package have ears which provide an insertion stop. Displays soldered into PC board holes 0.020" in diameter will have a nominal .080" space between the PC board and the back of the device. This space allows for air circulation. As with the connector mounted case, this space can be filled with heat sinking material if required.

HEAT SINKING

The 5082-7300 series are designed to operate with a maximum case temperature of 85°C, as measured at the back plane of the unit. Maintaining this temperature limit on the back plane or case will assure that the internal display temperature is within design limits. Case temperature can be measured with a small thermocouple connected to the case with thermally conductive compound.

When mounted in either a double DIP socket or soldered to a PC board, heat conduction through the display leads is typically adequate to maintain the case temperature to within 25°C of ambient.

Thus, in typical applications, the devices can be operated to an ambient of 60°C without external heat sinking.

In applications where the ambient temperature exceeds 60°C additional heat sinking is required. This can be achieved by use of a metallic strap normally mounted horizontally to the back plane of the display modules and the PC board or DIP socket. If adequate ventilation is not available, the metallic strap should be attached to an additional thermal conductor to provide good heat transfer. In addition, to assure a uniform thermal path between the display and the metal strap, a thermally conductive compound, such as Wakefield 120, or Dow Corning 340 should be used at this interface.

OPTICAL CONSIDERATIONS

The 5082-7300 series display modules are encapsulated with a contrast enhancing red filter. When the long-wave filter is cascaded with the spectral response of the eye, the composite response is that of a bandpass filter centered at approximately the peak of the light emitting diode spectrum. The filter enhances contrast by absorbing ambient light which impinges on the front surface of the display module. If additional filtering is desired, the use of Plexiglass #2423 is recommended. This inexpensive material offers contrast ratios in excess of 30/1, yet has transmissivity of 70% or better for the light emanated from the display.

Another filtering material is Polaroid HRCP-7, which combines a long wave pass filter like the Plexiglass, with a section of circularly polarized filtering material. Such a filter offers contrast ratios in excess of 100/1, but suffers from a transmissivity of only about 35% for the LED light. For reference, contrast ratio is defined as

$$C = \frac{S - N}{N}$$

where S is the luminance of the display elements, and N is the luminance of the background.

ELECTRICAL INTERFACE

The 5082-7300 series displays are fully DTL-TTL compatible. Each display decoder/driver includes a quad latch capable of storing 4 line BCD input data. In the 5082-7300/-7302, an additional bit of storage is provided for the decimal point input data. Utilizing this storage capability, the device will continue to display data after it is no longer available to the input.

The devices can also be used as a "real time" display (output at any time - only a function of the input at that time), by holding the enable line in the logic low state. Wiring pin 5 to ground potential is a convenient method of using the devices as real time displays.

When the latch feature is used, data should be available to the input 50ns or more before the enable rises to a Logic "1" level, and it should be held for 50ns or more after the enable rises to ensure reliable operation. The BCD inputs are positive logic and the decimal point convention is active low.

Except for the blanking control, all unused inputs may be left open or tied to V_{CC} through a resistor.

An unused blanking control input should be tied to ground.

The displays can be used with multi-digit data available in either bit parallel—character parallel or bit parallel—character serial format as illustrated in Figures 2 and 3 respectively. The 50ns setup time and 50ns hold time allows the data to be clocked into an array of displays at 10MHz.

Equivalent circuits for the logic, enable and blanking control inputs are shown in Figures 4 and 5.

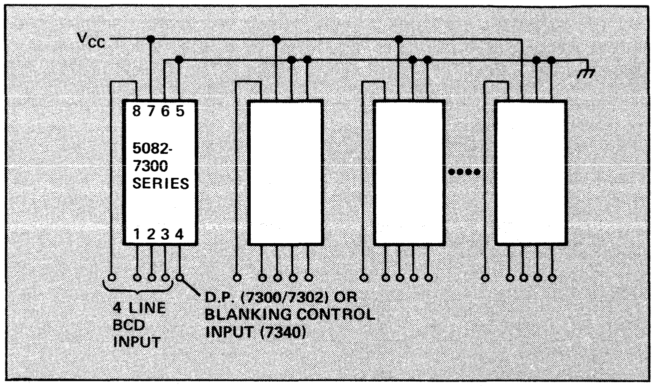


Figure 2. Bit Parallel, Character Parallel Wiring Configuration

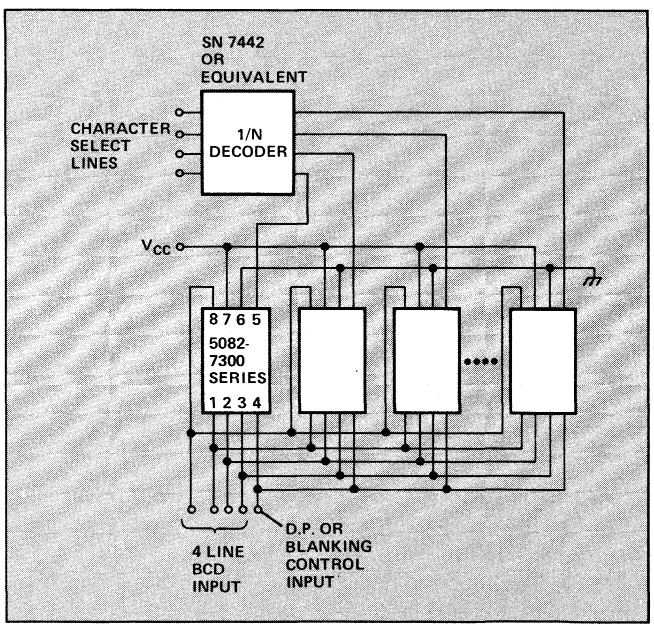


Figure 3. Bit Parallel, Character Serial Wiring Configuration

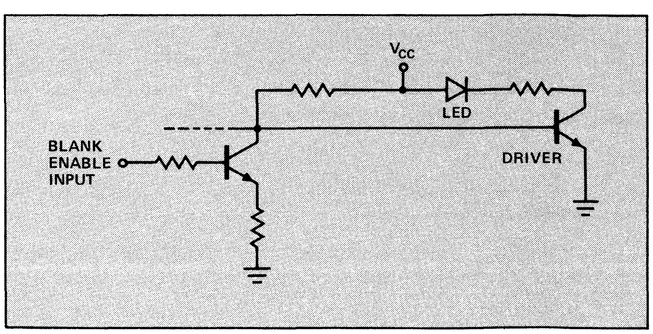


Figure 4. Equivalent Circuit of 7340 Blank Enable Input

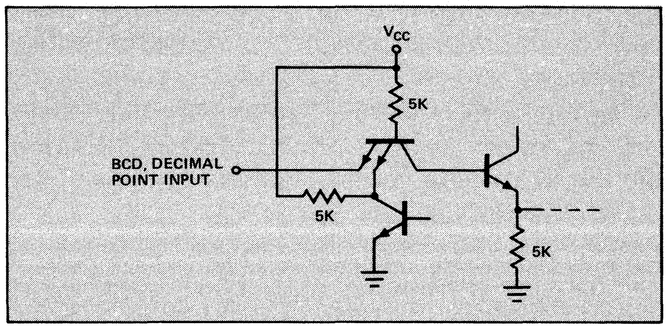


Figure 5. Equivalent Circuit of 7300/7302/7340 BCD, D.P., and Enable Inputs

BLANKING THE DISPLAY FOR INTENSITY CONTROL

The 5082-7300 series display modules can be blanked in several ways:

1. Applying a 3.5V min. signal to the -7340's blanking control input.
2. Applying one of the -7300/-7302's four BCD combinations which result in a blanked display.
3. Removing V_{CC} from the display module to be blanked.

Repetitive duty factor blanking by any of these methods can be used to decrease the apparent intensity of the display. If pulse width modulation is applied at a repetition rate of 100Hz or faster, the display will appear flicker free. This PWM technique can be used to control intensity over several orders of magnitude.

In Method 1, the -7340 replaces the decimal point input with a blanking control. Thus, method one allows the retention of the latched data and is the easiest to implement if the application does not require a decimal point. To interface DTL-TTL gates with the blanking control, a 3.3KΩ pull-up resistor should be connected between the blanking control input and V_{CC}. This assures that the 3.5V threshold will be reached when the driving gate's output is high.

Method 2 can be accomplished with 4 dual input OR gates per display as shown in Figure 6. The

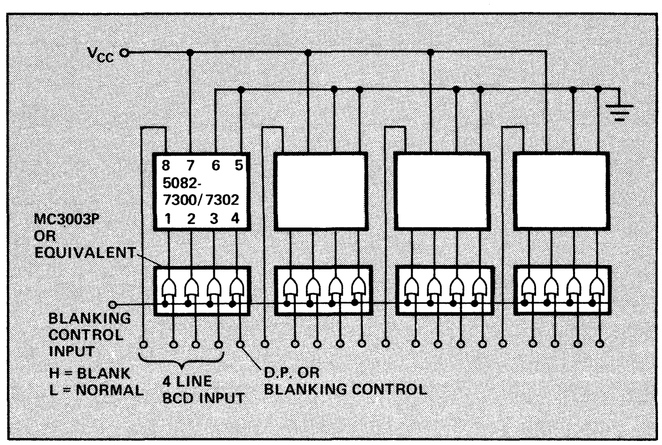


Figure 6. Bit Parallel, Character Parallel Blanking Scheme

I_{CC} current drawn by a display module when blanked by methods one or two is approximately 45 mA.

As an alternative, method 2 utilizes the uncommitted feature of "tri-state" logic. Figure 7 illustrates the use of tri-state decade counters with the 5082-7300/7302 displays.

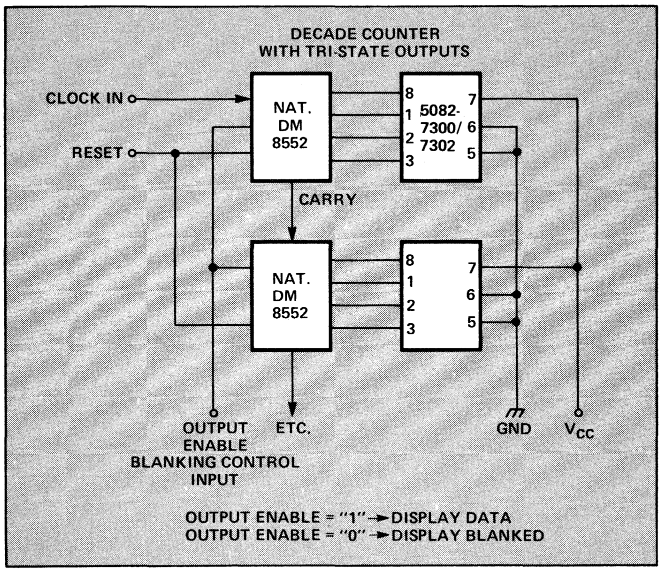


Figure 7. Blanking Scheme Example Using "Tri-State" Output Devices

When the outputs are "disabled", the BCD inputs to the display are effectively in the logic "1" state since no current can flow out of the input terminals.

Method 3 can be implemented as shown in Figure 8 by placing a switching transistor in the V_{CC} line. A cluster of display modules can be switched with one transistor. The transistor and power supply voltage should be chosen to keep the V_{CC} pin potential within the recommended range (4.5 to 5.5V).

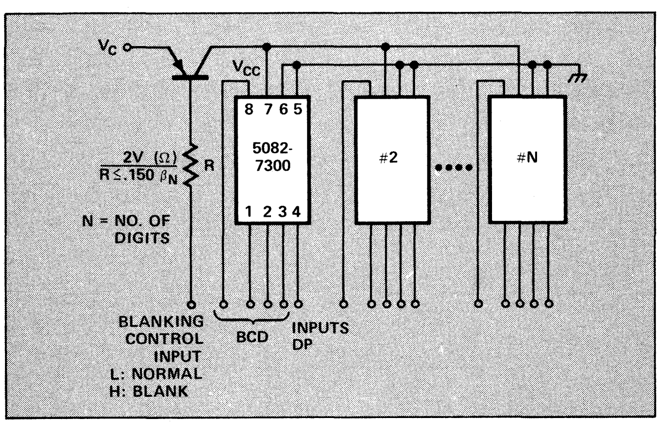


Figure 8. Blanking Using V_{CC} Line Switching

If this method is used, it is important that the V_{CC} pin not be connected to ground through a low resistance when any of the input lines (BCD, decimal point, enable) are held at a high voltage.

This method allows power saving for low levels of brightness, since no power is dissipated in the display modules when the device is in the "blanked" mode. However, the contents of the memory are lost whenever the V_{CC} line is cut off.

For brightness control, any of these blanking schemes can be used with a pulse width modulation circuit of the type shown in Figure 9.

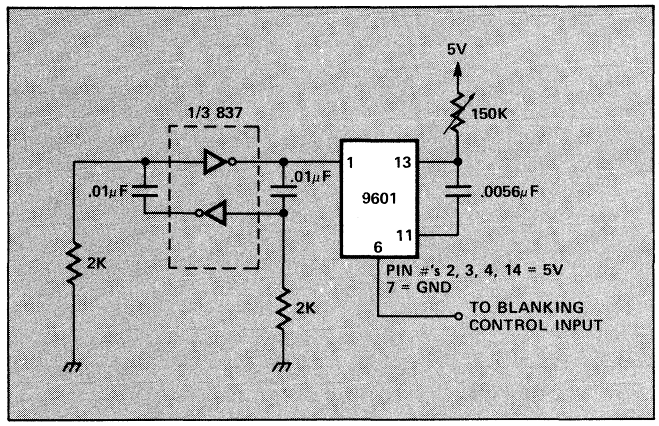


Figure 9. PWM Brightness Control Circuit

ACTIVATING THE DECIMAL POINT

The decimal point convention is "active low", i.e., low logic level corresponds to decimal point on. Hence, in normal applications where the probability of a decimal point being on is less than .5, this convention minimizes leakage current. In addition, the convention allows the decimal point pin to be left open when not used, and also allows use of an active low 1/N decoder, as described in Figure 10, to select the appropriate decimal point in "floating decimal point" applications.

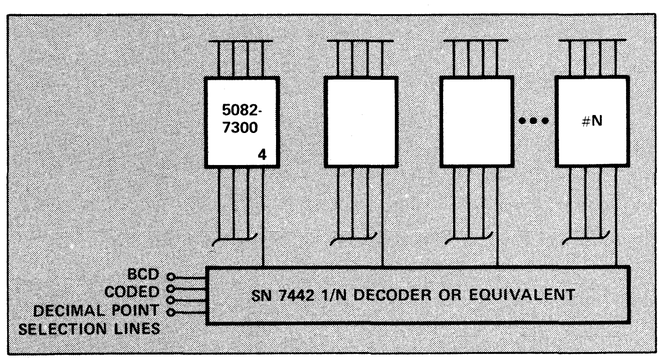
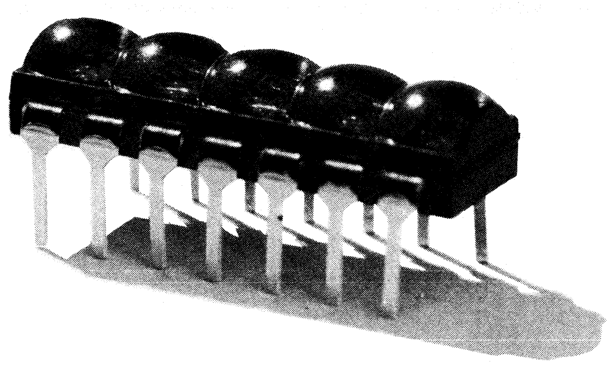


Figure 10. Activating Decimal Points with A 1/N Decoder.

HEWLETT PACKARD

COMPONENTS



APPLICATION NOTE 937

Monolithic Seven Segment LED Display Installation Techniques

INTRODUCTION

Hewlett-Packard offers a series of small, endstackable solid state displays for numeric and selected alphabetic character displays. These monolithic GaAsP displays, requiring as little as 7 mW per digit under pulsed operation, are highly readable at arm's length and lend themselves well to hand-held, portable applications. With all solid state construction, these displays are rugged and can be operated in severe environments.

The 7400 series is available in 3, 4, and 5 digit endstackable clusters. They can be used to form registers of 3 or more digits. These displays are available with the decimal point located either at the lower right of the digit or centered for use when the decimal point occupies a full digit position.

The displays are designed for strobing, a drive method that allows timesharing of the character generator among the digits in a display so that only 8 + N lead connections need be made to the display cluster for N characters.

This Application Note begins with an explanation of the strobing technique, followed by a discussion of the uses and advantages of the right hand and center decimal point products.

Several circuits are given for typical applications. Finally, a discussion of interfacing to various data forms is presented along with comments on mounting the displays.

DRIVE TECHNIQUES

Two general techniques can be used to drive seven segment displays in which the decoding function is performed externally to the display cluster. In strobed operation, the decoder is timeshared among the digits in the display, which are illuminated one at a time at a rate high enough to appear flicker-free (100Hz for most applications). In non-strobed operation, the display is operated with each character continuously illuminated, usually with one decoder per character. In addition to reducing the number of decoders and drivers, strobing requires less power than dc drive to achieve the same dis-

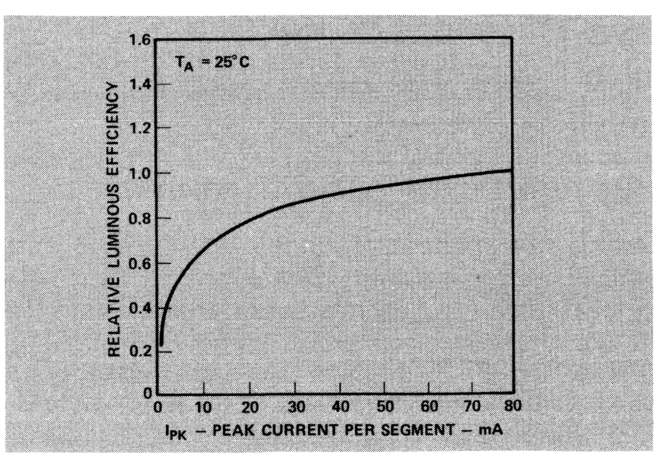


Figure 1. Relative Luminous Efficiency vs. Peak Current Per Segment.

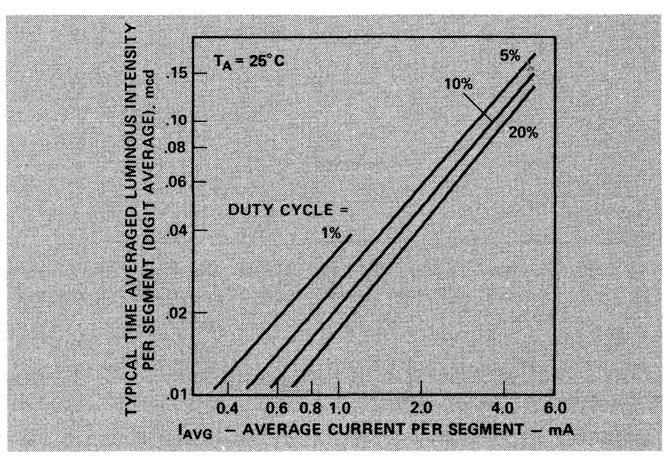


Figure 2. Typical Time Averaged Luminous Intensity per Segment (Digit Average) vs. Average Current per Segment.

play brightness. Figure 1 shows how the relative luminous efficiency of a segment varies with the peak current level. Figure 2 illustrates that, for the same average current, use of lower duty cycles (and higher peak current levels) results in increased light output. Thus, to achieve an increase in the light output of the display, an increase in either the time averaged forward current or the peak current drive is required.

The 5082-7400 series displays are designed to take full advantage of the strobing technique. The segments are wired to be segment-addressable; only 8+N leads are required for each cluster (7+N if the decimal point is not used). In addition, more than one cluster can be strobed by paralleling like segment enable lines of each cluster.

In operation, the appropriate segment (anode) enable lines are activated for the character to be displayed, and one common (cathode) enable line is activated to select the proper digit location. The strobe then progresses to the next digit position, activating its common enable line and the appropriate segment enable lines for that position. Figure 3 shows a schematic of a display with the associated activating functions shown as switches. The resistors serve to limit the light emitting diode currents. They are placed in the segment enable lines instead of the common enable lines to prevent uneven current distribution among segments.

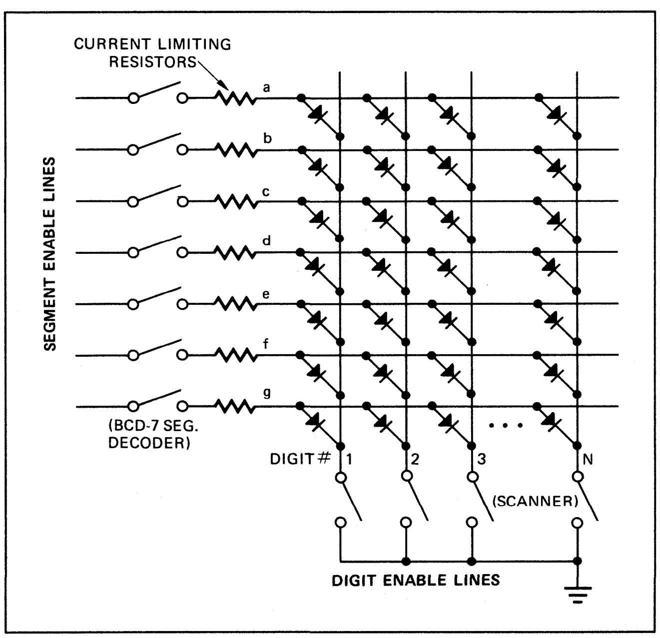


Figure 3. Schematic of 5082-7400 Series Displays, Shown With Current Limiting Resistors and Associated Switching Functions

The resistive current limiting approach for driving LED's outlined above is compact and easy to implement. However, the resistor consumes power. Figure 4a shows an idealized energy storage circuit, where the power wasting resistor is replaced

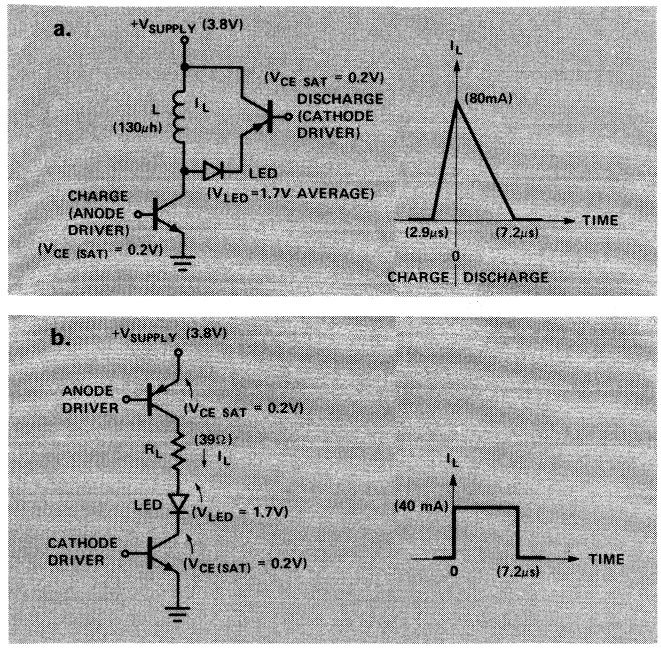


Figure 4: a. Inductive Drive Circuit, b. Resistive Drive Circuit

with an inductor, and shows a piece-wise linear approximation of the current waveform. This approach is attractive in battery powered applications. For example, the two simplified circuits of Figures 4a and 4b produce equal light output from a display, yet the inductive circuit consumes half the power of the resistive one. A disadvantage is that the inductive component can be space consuming for long pulse lengths. Thus, the method is typically used in high refresh rate applications (e.g., 100kHz). In addition, signal timing can be a problem. The capacitive analog to Figure 4a can also be used if provision is made to limit momentary current spikes to the safe level.

The intensity of the display can be varied with amplitude or pulse width modulation techniques. The latter is recommended for wide range brightness control. Pulse width modulation offers the advantage of good tracking between segments as the brightness is decreased, and also allows the LEDs to operate with a high peak current, where they are more efficient than low level DC drive. One technique is to control the duty cycle of the character illumination by use of a monostable multivibrator triggered by the display clock.

THE RIGHT-HAND DECIMAL POINT

As mentioned above, the 5082-7400 Series is available in two decimal point configurations — one with a lower right-hand decimal point and one that has the centered decimal point. The -7412, -7413, -7414, and -7415 displays have the decimal point locateu at the lower right side of the digit. In addition to normal applications, these displays can be directly interfaced to the growing number of LSI arithmetic units which generate their own timing pulses

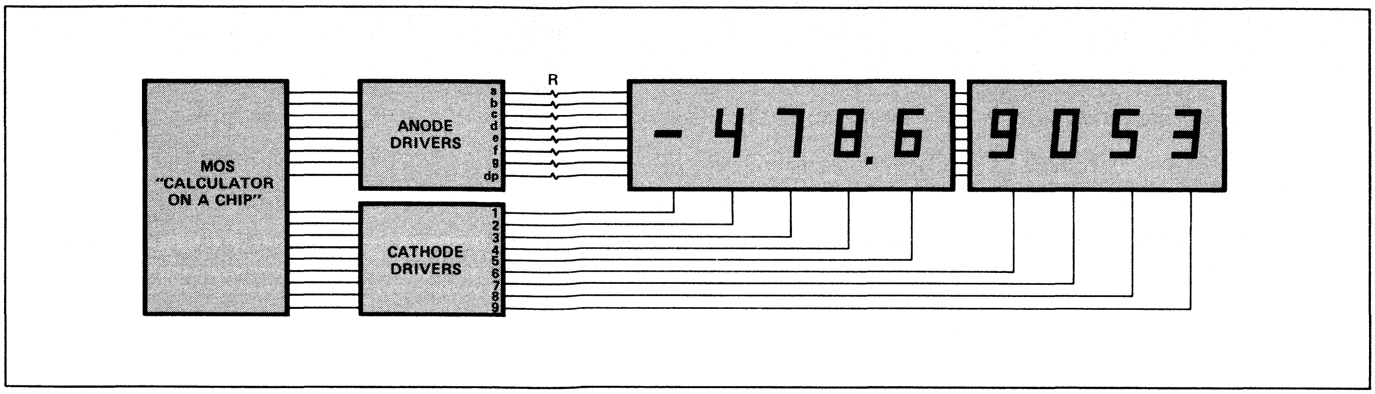


Figure 5a. Block Diagram for Calculator Display using Lower Right Decimal Point.

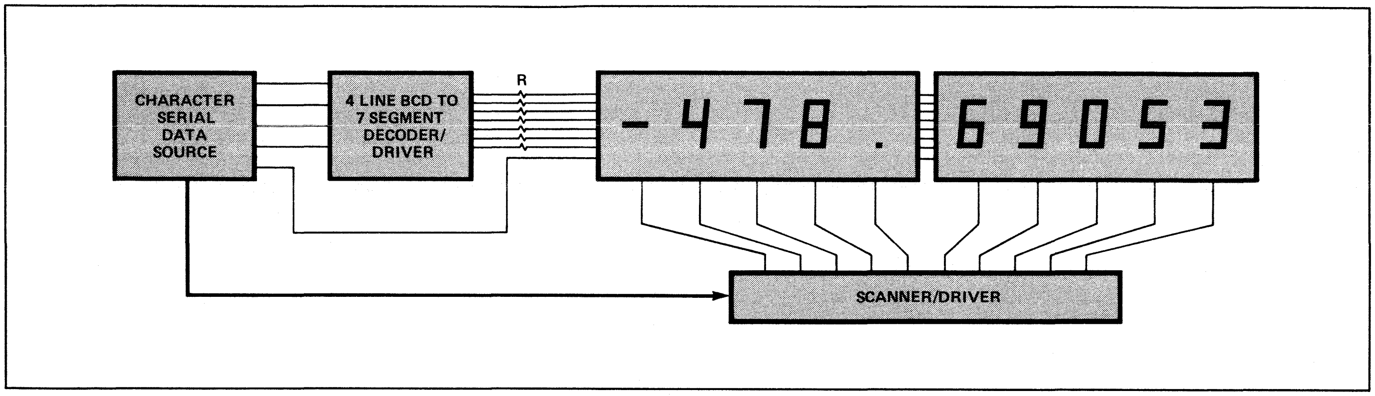


Figure 5b. Block Diagram for Display Using Center Decimal Point.

for data display. A typical block diagram of this approach is shown in Figure 5a where only the drive stages are needed to interface a MOS one chip calculator circuit to the display clusters.

A calculator circuit appears in Figure 6 in which transistor arrays have been used for the driving stages. MOS one-chip calculator circuits available include the TMS 1802 from TI and the MK 5010P from Mostek. The required peak current level can be determined using Figure 2. In the example, the duty cycle is 1 of 9 or 11%. Assuming the calculator will be operated in an office environment where a light level of .03 mcd per segment provides sufficient contrast, Figure 2 indicates that one needs an average current of 1.3mA or a peak current of (9) (1.3mA) = 12mA peak per segment. As the display is strobed, each anode driver must source a peak current of 12mA. Since the same anode may be turned on in every digit position, the average anode driver current is also 12mA. The current limiting resistor R1 in Figure 6 determines the peak segment current and is equal to:

$$R_1 = (V_{SS} - V_{SAT_1} - V_{LED} - V_{SAT_2}) / I_{peak/segment}$$

$$= (7.2 - 0.5 - 1.6 - 1.2)\text{V}/12\text{mA} \cong 330\Omega$$

The cathode driver must be capable of sinking the current from all segments on a 1 of 9 duty cycle or (8) (12mA) = 96mA peak and 96/9 = 10.7mA average.

TI produces Darlington drivers specifically designed for display applications. The SN 75491 is a Quad Segment Driver capable of sourcing 50mA per stage while the SN 75492 is a Hex Digit Driver able to sink 250mA per stage. Transistor arrays can also be used. Table 1 lists some of the arrays available.

The choice between Darlington arrays, transistor arrays, and discrete transistors depends upon the calculator manufacturers' relative component and assembly costs, as well as the current gain required by the particular circuit.

A useful circuit when a counter is required is Mostek's MK5002P 4 decade counter/decoder which provides, in addition to a counting circuit, all the decoding and timing needed to strobe four decades of display. These circuits can be ganged to provide greater than 4 decades of counting and display capacity.

THE CENTER DECIMAL POINT

In some applications such as printing calculators, existing timing circuitry makes it desirable to dedicate a digit position for decimal point display. In other applications, the decimal point in long display registers becomes hard to read because of the close spacing between the typical right hand decimal point and the character. Here the technique of dedicating a full digit position for decimal point display can improve both the recognition speed and accuracy. Designed for these applications, the

Manufacturer and No.	Configuration	Drive Stages per DIP	Peak I_c per Stage
Sprague ULN-2081A	NPN Common Emitter	7	200 mA
Sprague ULN-2082A	NPN Common Collector	7	200 mA
RCA CA 3081	NPN Common Emitter	7	100 mA
RCA CA 3082	NPN Common Collector	7	100 mA
RCA CA 3083	NPN Transistors	5	100 mA

Table I. Transistor Arrays

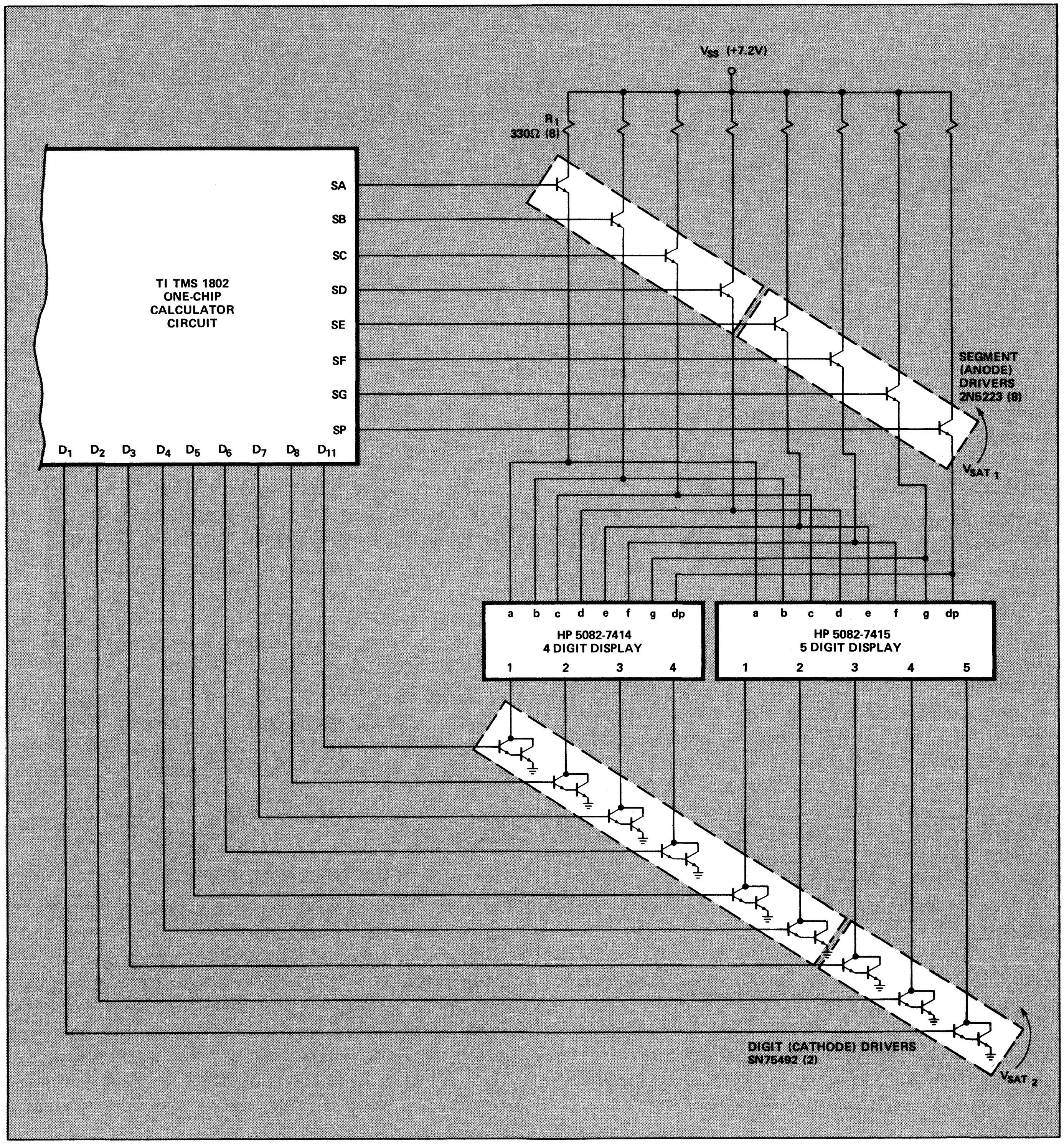


Figure 6. One-Chip Calculator Interface for Right Hand Decimal Displays.

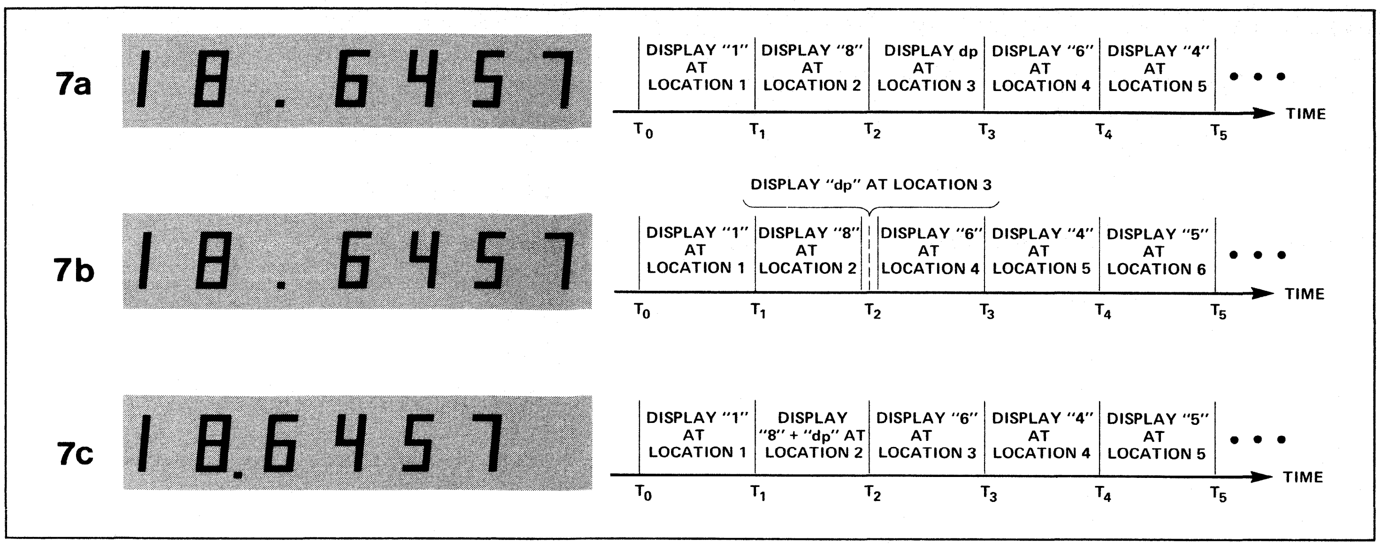


Figure 7. Decimal Point Display Techniques.

-7402, -7403, -7404, and -7405 displays contain a centrally located decimal point which is activated in place of a digit. A typical display system for this technique is outlined in Figure 5b.

In applications such as for printing calculators, a time frame as well as a digit position is dedicated to decimal point display (Figure 7a). For comparison, Figure 7c shows the technique normally used with a lower right decimal point. For other applications where a dedicated decimal point is desired, and one has the freedom of a custom design, this is often the easiest timing mode to implement. If one must interface to standard timing circuitry, the decimal point can be squeezed between two time frames while character information is steered to the proper slot. A timing diagram of this approach appears in Figure 7b. For the display to remain uniformly bright from character to character, the decimal point can consume only a small portion of the adjacent character's display time. To compensate for its much shorter pulse length, the decimal point's anode driver is usually designed to pulse at a higher current level, while the other anode drivers are momentarily disabled. A block diagram of this circuitry is shown in Figure 8. For character information appearing to the left of the decimal point, the Digit Select Steering Circuit steers digit timing signals without change. For character information following the decimal point, the i^{th} digit timing signals are steered to the (i^{th} + 1) cathode driver.

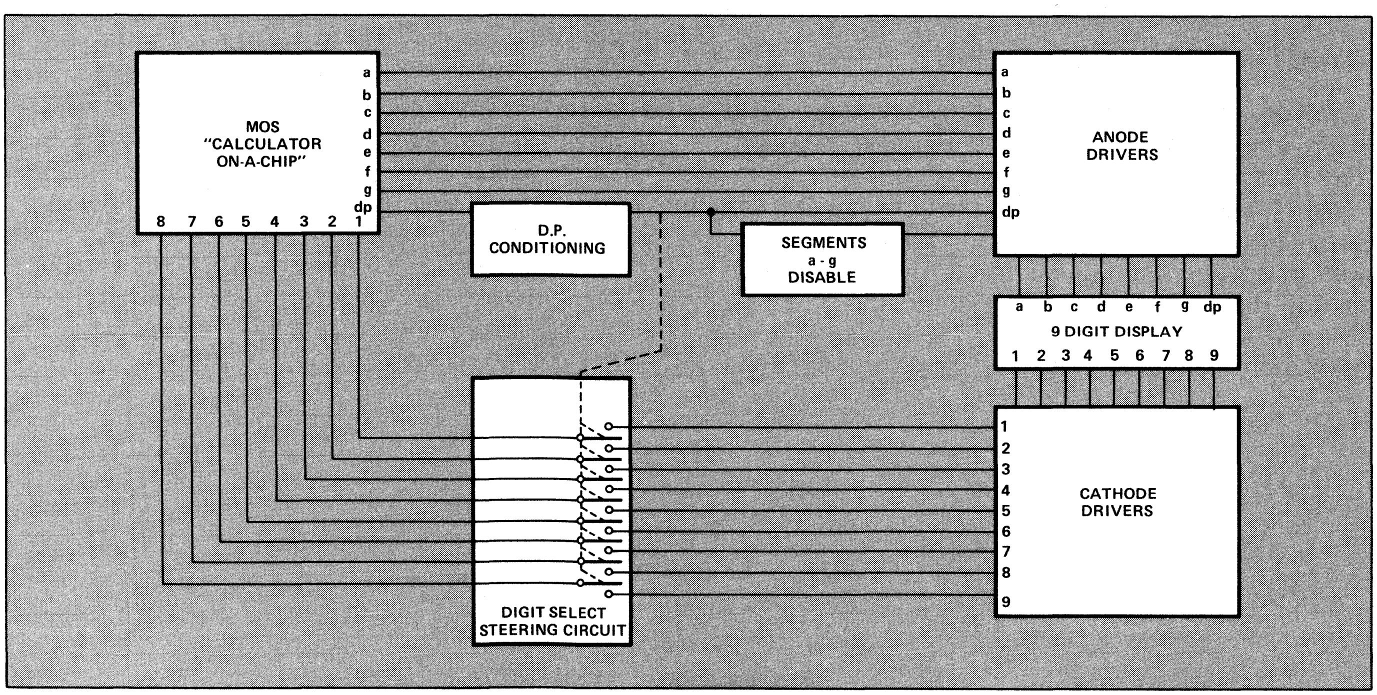


Figure 8. Block Diagram of Interface with Standard Timing Circuits.

INTERFACING TO VARIOUS DATA FORMS

The cluster approach to packaging is best suited to accept decoded bit parallel, character serial data. However, other data forms can be easily accommodated. If the data is bit parallel, character serial but coded into BCD form, a simple BCD-7 segment decoder is used. If the information arrives bit parallel, character parallel, a dynamic shift register can provide the recirculating memory to convert to a character serial format. An alternative is to use storage buffers, such as National's 8551 or equivalent, with the output enable lines tied to the digit select lines. As above, if the incoming data is in BCD form, a decoder should be inserted preceding the display. For fully serialized data, a serial in, parallel out shift register does the necessary conversion to character serial, bit parallel.

INTENSITY UNIFORMITY

The clusters are categorized for light output intensity such that the variation within one cluster is not discernible to the eye. Luminous intensity categories are designated by a letter located on the reverse side of the package. In multi-cluster applications, display appearance will be optimized when a given display uses clusters from a single category.

CONTRAST ENHANCEMENT

The background of the display and the type of contrast enhancing filter used strongly affect the quality of the perceived display. Typically, standard PC board mounting and a Plexiglass 2423 low pass filter is used. The contrast can be further improved by use of a circular polarizing filter (such as Polaroid's HRCP-Red). Anti-glare coatings are available to reduce filter surface reflections.

MOUNTING CONSIDERATIONS

A well designed instrument has the display mounted so its image plane is normal to the most frequent viewing angle. For hand-held or desk top applications, this usually means tilting the display at some angle to the instrument's main PC board. The desired orientation can be achieved by either mounting the display at an angle to the PC board or by tilting a portion of the board. The former may require more elaborate assembly fixturing, while the

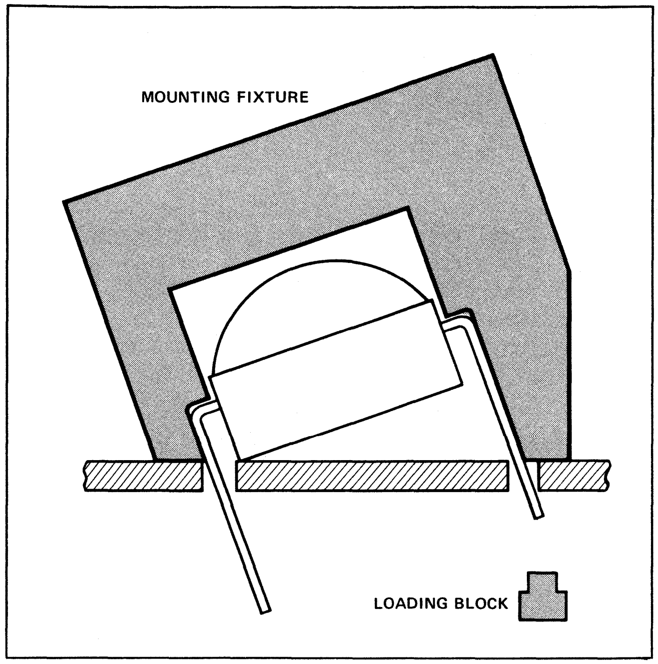


Figure 9. Mounting Fixture

latter can involve an additional PC board for the display which is then attached at the proper angle to the main board. In the HP display, the shoulders of the lead frame pins are intentionally raised above the bottom of the package, so that the display can be mounted at an angle to the PC board. Mounting angles up to 20° are easily accommodated.

A simple and easy-to-use fixture (fabrication drawings available from Hewlett-Packard) is shown in Figure 9, which functions both as an alignment aid and an insertion tool. It also serves as an excellent heat sink required for most wave soldering operations. Designed to mount a 3 cluster register at a 20° tilt, this fixture eliminates the requirement for a separate tilted PC board and can be adapted for applications involving other tilt angles and register lengths. The procedure is to snap the fixture over clusters which have been placed on the loading block. After using the fixture to aid PC board insertion, the tool holds the clusters in the proper position during wave solder and is then removed. The 5082-7400 series can be soldered into the PC board at a maximum soldering temperature of 260°C for 5 seconds.

HEWLETT PACKARD COMPONENTS

APPLICATION BRIEF

5082-7730 Series Seven Segment Display

INTRODUCTION

Hewlett-Packard offers the 5082-7730 series of 0.3" high single digit seven segment LED displays for a wide range of instrument, calculator and business applications. The devices display numeric and selected alphabetic character information. Packaged in a standard DIP package, these units employ a new optical magnification technique which converts seven discrete LED chips into seven large uniformly intense bars readable at 10 feet. With all solid state construction, these devices are rugged and can be operated in severe environments.

The 7730 series is available in two configurations. The 7730 is a common anode display employing a left-hand decimal point for applications such as electronic instrumentation, computer systems, and business machines, among others. The common anode 7731 utilizes a right-hand decimal point for applications that include electronic calculators and business terminals such as credit card verifiers.

The 5082-7730 and 7731 devices use only one LED per segment providing a 1.6V typical forward voltage. If your product design employs displays with two series LEDs per segment (for a 3.4V forward voltage), you will need to increase the value of the current limiting resistor. The formulas mentioned under the DC and Strobed Drive sections can be used to determine the new resistor value.

DC DRIVE

In DC or non-strobed drive the display is operated with each character continuously illuminated, usually with one decoder per character. This technique is commonly used for short character strings where the cost of the decoders for DC drive is less than that for the timing and drive circuits of strobed operation. The LEDs are more efficient when strobed; however, in DC operation the drivers need not handle high current levels. The DC drive circuit for the common anode display is shown in Figure 1. The current level, set here at 20mA per segment, is determined by the relation

$$R = \frac{V_{CC} - V_{LED} - V_{ON}}{I_{SEGMENT}}$$

where V_{CC} = Voltage supply potential, V_{LED} = forward voltage of LED at $I_{SEGMENT}$, V_{ON} = driver output voltage at $I_{SEGMENT}$, and $I_{SEGMENT}$ = desired operating current in each segment.

Commercially available 7 segment decoder/driver circuits include the TI SN7447A, Motorola MC 4309, Fairchild 9317B and C, CMI 5110 and 5111 (includes latch), and SCS 1001. The latter circuit is a hybrid able to sink 120mA per segment.

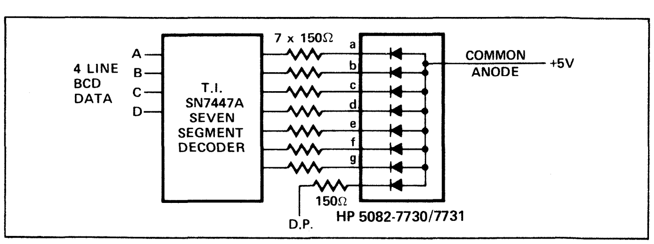


Figure 1. Direct Drive Circuit for the 5082-7730/7731 Common Anode Display.

STROBING DRIVE CIRCUITS

In strobing, the decoder is timeshared among the digits in the display, which are illuminated one at a time at a rate high enough to appear flicker-free. 100Hz is adequate for most applications; however, if the display is subject to vibration, the strobe rate should be 5 times the maximum vibration rate. This assures that the perceived display is continuous and easy to read. The digits are electrically connected with the enable lines of like segments hooked in parallel. This forms an 8 (7 segments and decimal point) x N (number of digits) array. In operation, the appropriate segment enable lines are activated for the particular character to be displayed. At the same time a common enable line is selected so that the character appears at the proper digit location. The strobe then progresses to the next digit position, activating the proper segments and common enable line for that position.

In addition to reducing the number of decoders and drivers, strobing requires less power than DC drive to achieve the same display intensity. This is due to a basic property of GaAsP where relative efficiency (luminous intensity/unit current) increases with the peak current level. Thus, for the same average current, use of lower duty cycles (and higher peak current levels) results in increased light output.

A series resistor is placed in each segment enable line to limit the light emitting diode current. They are placed in the segment enable lines instead of the common enable lines to prevent uneven current distribution among segments, commonly referred to as "current hogging".

Figure 2 depicts a 5-digit strobed display employing a recirculating shift register memory. One shift register is used for each bit of the 4-bit BCD code. Four lines of data from the shift registers drive an SN7447A seven-segment decoder. The value of the current limiting resistors is calculated to provide 50mA per segment peak drive current. The resistor value may be calculated using the following formula:

$$R = \frac{V_{CC} - V_{LED} - V_{CE1} - V_{CE2}}{N\,I_{AVE}}$$

where V_{CC} = voltage supply potential, V_{LED} = forward voltage of LED at peak $I_{SEGMENT}$ ($N\,I_{AVE}$), V_{CE1} = "ON" voltage of segment switch at peak $I_{SEGMENT}$, V_{CE2} = "ON" voltage of digit switch at 8 times peak $I_{SEGMENT}$, I_{AVE} = desired average operating current per segment, and N = number of digits on the display.

Data for each digit of the display is sequentially shifted to the Q_E output of the shift register by the display scan clock. The scan clock also drives an SN7496 shift register set up as a ripple scanner. The scan shift register outputs are buffered to source the 400mA peak digit current. Data entry to the storage registers is controlled by the system clock of the data source. During data entry, the display is blanked and the scan shift register is reset to position "A" with a logic "0" at $\overline{\text{DATA ENTER}}$. The DATA SOURCE SYSTEM CLOCK and the external BCD lines are also enabled by $\overline{\text{DATA ENTER}}$. The 5 digits of new data will be entered

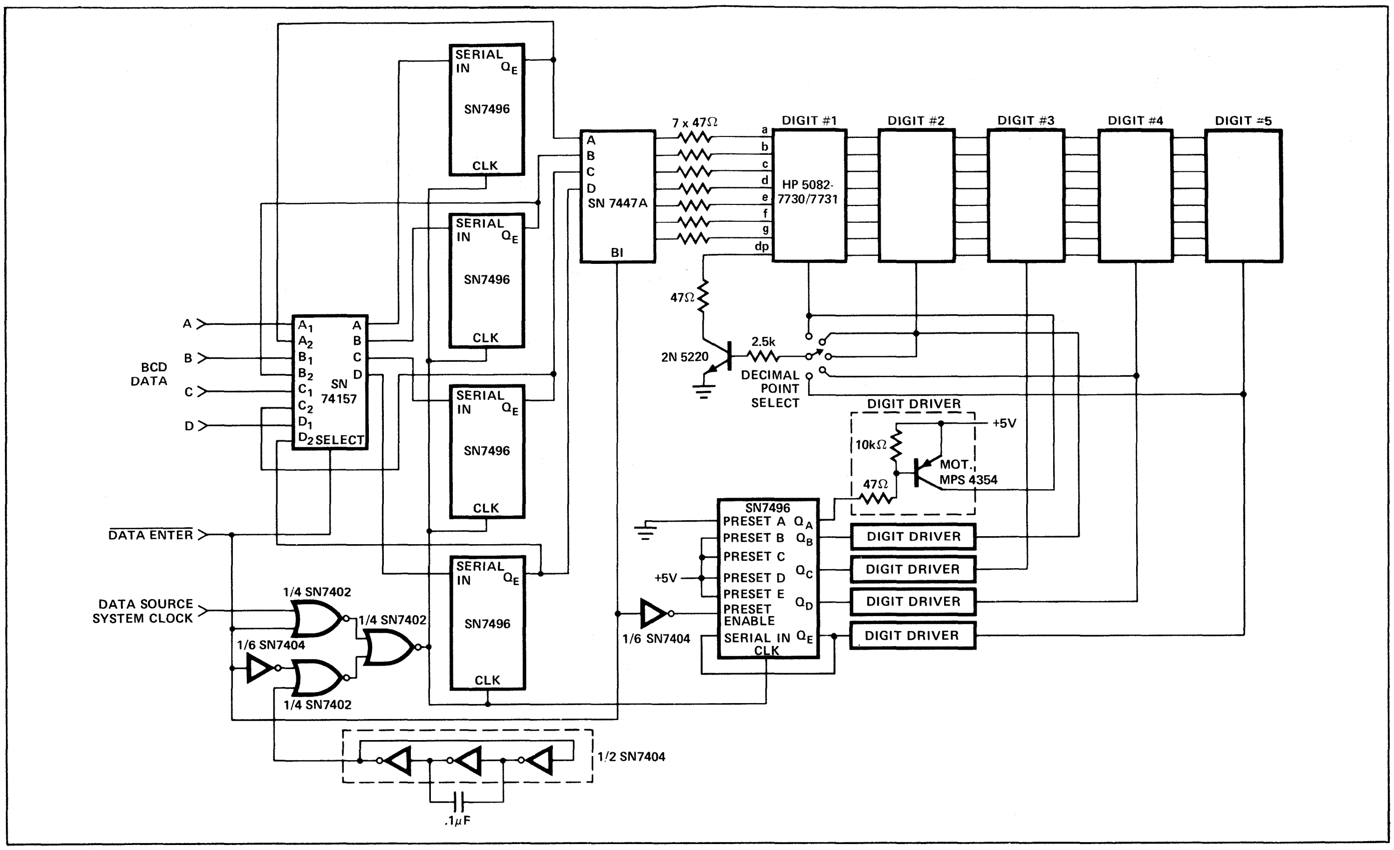


Figure 2. Five Digit Strobed Display with Recirculating Shift Register Memory.

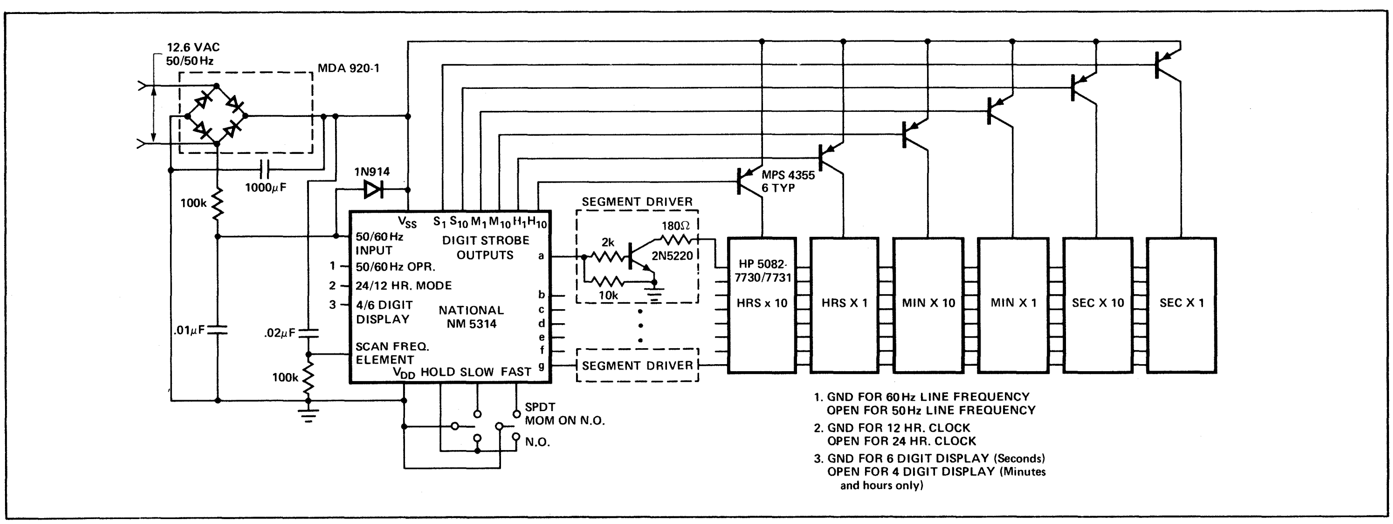


Figure 3. Strobed Drive for a Six Digit Clock.

into the shift registers on each positive transition of the system clock. After data entry, $\overline{\text{DATA ENTER}}$ is returned to a high state, and scanning begins at position "A" under control of the SCAN CLOCK.

CLOCKS

Figure 3 illustrates a 6-digit clock using the National Semiconductor MM5314 clock chip. This chip uses a strobed technique with all scanning logic and memory buffers on board. Scan frequency is established by an external RC network and should be maintained between 600 Hz and 10 kHz. The values shown should generate approximately a 1 kHz scan rate. Each of the P-channel MOS outputs are buffered to provide adequate drive current to the individual segment and digit enable lines.

MOUNTING CONSIDERATIONS

The 5082-7730 and 5082-7731 devices are constructed utilizing a lead frame in a standard DIP package. In addition to easy PC board mounting, the standard pin spacing of .100" between pins and .300" between pin rows allows use of the familiar 14 pin IC sockets. The displays may be end-stacked as close as .400" center-to-center. The lead frame has an integral seating plane which holds the package approximately .045" above the PC board during standard soldering and flux removal operations. The devices can be soldered for up to 5 seconds at a maximum solder temperature of 230°C (1/16" below the seating plane). To optimize device performance, new materials are used that are limited to certain solvent materials for flux removal. It is recommended that only Freon TF or Isopropanol be used for cleaning operations.

NOTES:

NOTES:

Distributor Stocking Locations

HALL-MARK ELECTRONICS

Huntsville, Alabama
205/539-0691

Raleigh, North Carolina
919/832-4465

Houston, Texas
713/781-6100

Lenexa, Kansas
913/888-4747

Tulsa, Oklahoma
918/835-8458

St. Louis, Missouri
314/521-3800

Dallas, Texas
214/231-6111

SCHWEBER ELECTRONICS

Hollywood, Florida
305/927-0511

Rockville, Maryland
301/881-2970

Westbury, New York
516/334-7474

Toronto, Ontario, Canada
416/925-2471

Elk Grove Village, Illinois
312/593-2740

Waltham, Massachusetts
617/890-8484

Somerset, New Jersey
201/469-6008

Troy, Michigan
313/583-9242

Rochester, New York
716/328-4180

Beachwood, Ohio
216/464-2970

WYLE DISTRIBUTION GROUP

Liberty Electronics/Arizona
Phoenix, Arizona
602/257-1272

Western Radio
San Diego, California
714/235-6571

Liberty Electronics
El Segundo, California
213/322-8100

Elmar Electronics
Commerce City, Colorado
303/287-9611

Elmar Electronics
Mtn. View, California
415/961-3611

Liberty Electronics/N.W.
Seattle, Washington
206/763-8200

EUROPEAN

Celdis Ltd.
37-39 Loverock Rd., Reading
Berks, England
Tel: READING 58 22 11

Ingenieurburo Dreyer
238 Schleswig
Flensburger Strasse 3
West Germany
Tel: (04621) 2 31 21

B.V. Diode
Hollantlaan 22
Utrecht City
The Netherlands
Tel: (030) 88 42 14

EBV Elektronik
8 Munich 2
Gabriel-Max-Strasse 90
West Germany
Tel: (0811) 644055-8

Interelko A.B.
Sandsborgsvagen 50
12 233 Enskede
Sweden
Tel: (08) 49 25 05

EBV Elektronik
6 Frankfurt/Main 1
Myliusstrasse 54
West Germany
Tel: (0611) 720416-18

I.S.C. France
20 rue Gambetta
92-Boulogne
France
Tel: 604.52.75

SALES & SERVICE OFFICES

UNITED STATES

ALABAMA
P.O. Box 4207
2003 Byrd Spring Road S.W.
Huntsville 35802
Tel: (205) 881-4591
TWX: 810-726-2204

ARIZONA
2336 E. Magnolia St.
Phoenix 85034
Tel: (602) 252-5061
TWX: 910-951-1330

5737 East Broadway
Tucson 85716
Tel: (602) 298-2313
TWX: 910-952-1162

CALIFORNIA
1430 East Orangethorpe Ave.
Fullerton 92631
Tel: (714) 870-1000

3939 Lankershim Boulevard
North Hollywood 91604
Tel: (213) 877-1282
TWX: 910-499-2170

1101 Embarcadero Road
Palo Alto 94303
Tel: (415) 327-6500
TWX: 910-373-1280

2220 Watt Ave.
Sacramento 95825
Tel: (916) 482-1463
TWX: 910-367-2092

9606 Aero Drive
San Diego 92123
Tel: (714) 279-3200
TWX: 910-335-2000

COLORADO
7965 East Prentice
Englewood 80110
Tel: (303) 771-3455
TWX: 910-935-0705

CONNECTICUT
12 Lunar Drive
New Haven 06525
Tel: (203) 389-6551
TWX: 710-465-2029

FLORIDA
P.O. Box 24210
2806 W. Oakland Park Blvd.
Ft. Lauderdale 33307
Tel: (305) 731-2020
TWX: 510-955-4099

P.O. Box 13910
6177 Lake Ellenor Dr.
Orlando, 32809
Tel: (305) 859-2900
TWX: 810-850-0113

GEORGIA
P.O. Box 28234
450 Interstate North
Atlanta 30328
Tel: (404) 436-6181
TWX: 810-766-4890

HAWAII
2875 So. King Street
Honolulu 96814
Tel: (808) 955-4455

ILLINOIS
5500 Howard Street
Skokie 60076
Tel: (312) 677-0400
TWX: 910-223-3613

INDIANA
3839 Meadows Drive
Indianapolis 46205
Tel: (317) 546-4891
TWX: 810-341-3263

LOUISIANA
P.O. Box 856
1942 Williams Boulevard
Kenner 70062
Tel: (504) 721-6201
TWX: 810-955-5524

MARYLAND
6707 Whitestone Road
Baltimore 21207
Tel: (301) 944-5400
TWX: 710-862-9157

P.O. Box 1648
2 Choke Cherry Road
Rockville 20850
Tel: (301) 948-6370
TWX: 710-828-9684

MASSACHUSETTS
32 Hartwell Ave.
Lexington 02173
Tel: (617) 861-8960
TWX: 710-326-6904

MICHIGAN
21840 West Nine Mile Road
Southfield 48075
Tel: (313) 353-9100
TWX: 810-224-4882

MINNESOTA
2459 University Avenue
St. Paul 55114
Tel: (612) 645-9461
TWX: 910-563-3734

MISSOURI
11131 Colorado Ave.
Kansas City 64137
Tel: (816) 763-8000
TWX: 910-771-2087

148 Weldon Parkway
Maryland Heights 63043
Tel: (314) 567-1455
TWX: 910-764-0830

NEW JERSEY
W. 120 Century Road
Paramus 07652
Tel: (201) 265-5000
TWX: 710-990-4951

1060 N. Kings Highway
Cherry Hill 08034
Tel: (609) 667-4000
TWX: 710-892-4945

NEW MEXICO
P.O. Box 8366
Station C
6501 Lomas Boulevard N.E.
Albuquerque 87108
Tel: (505) 265-3713
TWX: 910-989-1665

156 Wyatt Drive
Las Cruces 88001
Tel: (505) 526-2485
TWX: 910-983-0550

NEW YORK
6 Automation Lane
Computer Park
Albany 12205
Tel: (518) 458-1550
TWX: 710-441-8270

1219 Campville Road
Endicott 13760
Tel: (607) 754-0050
TWX: 510-252-0890

82 Washington Street
Poughkeepsie 12601
Tel: (914) 454-7330
TWX: 510-248-0012

39 Saginaw Drive
Rochester 14623
Tel: (716) 473-9500
TWX: 510-253-5981

5858 East Molloy Road
Syracuse 13211
Tel: (315) 454-2486
TWX: 710-541-0482

1 Crossways Park West
Woodbury 11797
Tel: (516) 921-0300
TWX: 510-223-0811

NORTH CAROLINA
P.O. Box 5188
1923 North Main Street
High Point 27262
Tel: (919) 885-8101
TWX: 510-926-1516

OHIO
25575 Center Ridge Road
Cleveland 44145
Tel: (216) 835-0300
TWX: 810-427-9129

3460 South Dixie Drive
Dayton 45439
Tel: (513) 298-0351
TWX: 810-459-1925

1120 Morse Road
Columbus 43229
Tel: (614) 846-1300

OKLAHOMA
6301 N. Meridian Avenue
Oklahoma City 73122
Tel: (405) 721-0200
TWX: 910-830-6862

OREGON
Westhills Mall, Suite 158
4475 S.W. Scholls Ferry Road
Portland 97225
Tel: (503) 292-9171
TWX: 910-464-6103

PENNSYLVANIA
2500 Moss Side Boulevard
Monroeville 15146
Tel: (412) 271-0724
TWX: 710-797-3650

1021 8th Avenue
King of Prussia Industrial Park
King of Prussia 19406
Tel: (215) 265-7000
TWX: 510-660-2670

RHODE ISLAND
873 Waterman Ave.
East Providence 02914
Tel: (401) 434-5535
TWX: 710-381-7573

***TENNESSEE**
Memphis
Tel: (901) 274-7472

TEXAS
P.O. Box 1270
201 E. Arapaho Rd.
Richardson 75080
Tel: (214) 231-6101
TWX: 910-867-4723

P.O. Box 27409
6300 Westpark Drive
Suite 100
Houston 77027
Tel: (713) 781-6000
TWX: 910-881-2645

231 Billy Mitchell Road
San Antonio 78226
Tel: (512) 434-4171
TWX: 910-871-1170

UTAH
2890 South Main Street
Salt Lake City 84115
Tel: (801) 487-0715
TWX: 910-925-5681

VERMONT
P.O. Box 2287
Kennedy Drive
South Burlington 05401
Tel: (802) 658-4455
TWX: 510-299-0025

VIRGINIA
P.O. Box 6514
2111 Spencer Road
Richmond 23230
Tel: (703) 285-3431
TWX: 710-956-0157

WASHINGTON
433-108th N.E.
Bellevue 98004
Tel: (206) 454-3971
TWX: 910-443-2303

***WEST VIRGINIA**
Charleston
Tel: (304) 768-1232

FOR U.S. AREAS NOT LISTED:
Contact the regional office nearest you: Atlanta, Georgia . . . North Hollywood, California . . . Paramus, New Jersey . . . Skokie, Illinois. Their complete addresses are listed above.

*Service Only

EUROPE

AUSTRIA
Hewlett-Packard Ges.m.b.H
Handelska 52/3
P.O. Box 7
A-1205 **Vienna**
Tel: (0222) 33 66 06 to 09
Cable: HEWPAK Vienna
Telex: 75923 hewpak a

BELGIUM
Hewlett-Packard Benelux
S.A./N.V.
Avenue du Col-Vert, 1
B-1170 **Brussels**
Tel: (02) 72 22 40
Cable: PALOBEN Brussels
Telex: 23 494

DENMARK
Hewlett-Packard A/S
Datavej 38
DK-3460 **Birkerod**
Tel: (01) 81 66 40
Cable: HEWPACK AS
Telex: 16640 hp as

Hewlett-Packard A/S
Torvet 9
DK-8600 **Silkeborg**
Tel: (06)-82-71-66
Telex: 16640 hp as
Cable: HEWPACKAS

FINLAND
Hewlett-Packard Oy
Bulevardi 26
P.O. Box 12185
SF-00120 **Helsinki** 12
Tel: (90) 13730
Cable: HEWPACKOY-Helsinki
Telex: 17-1563 hel

FRANCE
Hewlett-Packard France
Quartier de Courtaboeuf
Boite Postale No. 6
F-91401 **Orsay**
Tel: (1) 907 78 25
Cable: HEWPACK Orsay
Telex: 60048

Hewlett-Packard France
4 Quai des Etroits
F-69321 **Lyon Cedex** 1
Tel: (78) 42 63 45
Cable: HEWPACK Lyon
Telex: 31617

Hewlett-Packard France
29 rue de la Gare
F-31700 **Blagnac**
Tel: (61) 85 82 29
Telex: 51957

GERMAN FEDERAL REPUBLIC
Hewlett-Packard Vertriebs-GmbH
Berliner Strasse 117
Postfach 560 140
D-6 Nieder-Eschbach/Ffm 56
Tel: (0611) 50-04-1
Cable: HEWPACKSA Frankfurt
Telex: 41 32 49 FRA

Hewlett-Packard Vertriebs-GmbH
Herrenbergerstrasse 110
D-7030 **Böblingen**, Württemberg
Tel: (07031) 66 72 87
Cable: HEPAK Böblingen
Telex: 72 65 739 bbn

Hewlett-Packard Vertriebs-GmbH
Vogelsanger Weg 38
D-4 **Düsseldorf**
Tel: (0211) 63 80 31/35
Telex: 85/86 533 hpdd d

Hewlett-Packard Vertriebs-GmbH
Wendenstr. 23
D-2 **Hamburg** 1
Tel: (0411) 24 05 51/52
Cable: HEWPACKSA Hamburg
Telex: 21 53 032 hphh d

Hewlett-Packard Vertriebs-GmbH
Unterhachinger Strasse 28
ISAR Center
D-8012 **Ottobrunn**
Tel: (0811) 601 30 61/7
Telex: 52 49 85
Cable: HEWPACKSA Müchen

(West Berlin)
Hewlett-Packard Vertriebs-GmbH
Wilmersdorfer Strasse 113/114
D-1000 **Berlin W.** 12
Tel: (0311) 3137046
Telex: 18 34 05 hpbln d

GREECE
Kostas Karayannis
18, Ermou Street
Athens 126
Tel: 3230-303
Cable: RAKAR Athens
Telex: 21 59 62 rkar gr

IRELAND
Hewlett-Packard Ltd.
224 Bath Road
Slough, SL1 4 DS, Bucks
Tel: Slough (0753) 33341
Cable: HEWPIE Slough
Telex: 84413

Hewlett-Packard Ltd.
The Graftons
Stamford New Road
Altrincham, Cheshire, England
Tel: (061) 928-8626
Telex: 668068

ITALY
Hewlett-Packard Italiana S.p.A.
Via Amerigo Vespucci 2
1-20124 **Milan**
Tel: (2) 6251 (10 lines)
Cable: HEWPACKIT Milan
Telex: 32046

Hewlett-Packard Italiana S.p.A.
Piazza Marconi
1-00144 **Rome - Eur**
Tel: (6) 5912544/5, 5915947
Cable: HEWPACKIT Rome
Telex: 61514

Hewlett-Packard Italiana S.p.A.
Vicolo Pastori, 3
I-35100 **Padova**
Tel: (49) 66 40 62
Telex: 32046 via Milan

Hewlett-Packard Italiana S.p.A.
Via Colli, 24
I-10129 **Turin**
Tel: (11) 53 82 64
Telex: 32046 via Milan

LUXEMBURG
Hewlett-Packard Benelux
S.A./N.V.
Avenue du Col-Vert, 1
B-1170 **Brussels**
Tel: (03/02) 72 22 40
Cable: PALOBEN Brussels
Telex: 23 494

NETHERLANDS
Hewlett-Packard Benelux, N.V.
Weerdestein 117
P.O. Box 7825
Amsterdam, Z 11
Tel: 020-42 77 77
Cable: PALOBEN Amsterdam
Telex: 13 216 hepa nl

NORWAY
Hewlett-Packard Norge A/S
Box 149
Nesveien 13
N-1344 **Haslum**
Tel: (02)-53 83 60
Telex: 16621 hpnas n

PORTUGAL
Telectra-Empresa Tecnica de Equipamentos
Electricos S.a.r.l.
Rua Rodrigo da Fonseca 103
P.O. Box 2531
P-**Lisbon** 1
Tel: (19) 68 60 72
Cable: TELECTRA Lisbon
Telex: 1598

SPAIN
Hewlett-Packard Española, S.A.
Jerez No 8
Madrid 16
Tel: 458 26 00
Telex: 23515 hpe

Hewlett-Packard Española, S.A
Milanesado 21-23
E-**Barcelona** 17
Tel: (3) 203 62 00
Telex: 52603 hpbe e

SWEDEN
Hewlett-Packard Sverige AB
Enighetsvägen 1-3
Fack
S-161 20 **Bromma** 20
Tel: (08) 98 12 50
Cable: MEASUREMENTS Stockholm
Telex: 10721

Hewlett-Packard Sverige AB
Hagakersgatan 9C
S-431 41 **Mölndal**
Tel: (031) 27 68 00/01
Telex: 21 312 hpmindl s

SWITZERLAND
Hewlett Packard (Schweiz) AG
Zürcherstrasse 20
P.O. Box 64
CH-8952 **Schlieren** Zurich
Tel: (01) 98 18 21/24
Cable: HPAG CH
Telex: 53933 hpag ch

Hewlett-Packard (Schweiz) AG
Rue du Bois-du-Lan 7
P.O. Box 85
1217 Meyrin 2 **Geneva**
Tel: (022) 41 54 00
Cable: HEWPACKSA Geneva
Telex: 27333 hpsa ch

TURKEY
Telekom Engineering Bureau
Saglik Sok No. 15/1
Ayaspasa-Beyoglu
P.O. Box 437 Beyoglu
Istanbul
Tel: 49 40 40
Cable: TELEMATION Istanbul

UNITED KINGDOM
Hewlett-Packard Ltd.
224 Bath Road
Slough, SL1 4 DS, Bucks
Tel: Slough (0753) 33341
Cable: HEWPIE Slough
Telex: 84413

Hewlett-Packard Ltd.
"The Graftons"
Stamford New Road
Altrincham, Cheshire
Tel: (061) 928-8626
Telex: 668068

SOCIALIST COUNTRIES PLEASE CONTACT:
Hewlett-Packard Ges.m.b.H.
Handelskai 52/3
P.O. Box 7
A-1205 **Vienna**
Ph: (0222) 33 66 06 to 09
Cable: HEWPACK Vienna
Telex: 75923 hewpak a

ALL OTHER EUROPEAN COUNTRIES CONTACT:
Hewlett-Packard S.A.
Rue du Bois-du-Lan 7
P.O. Box 85
CH-1217 Meyrin 2 **Geneva**
Switzerland
Tel: (022) 41 54 00
Cable: HEWPACKSA Geneva
Telex: 2.24.86

AFRICA, ASIA, AUSTRALIA, CANADA, CENTRAL AND SOUTH AMERICA

MEDITERRANEAN AND MIDDLE EAST COUNTRIES CONTACT:
Hewlett-Packard
Co-ordination Office for Mediterranean and Middle East Operations
Via Marocco, 7
I-00144 Rome-Eur, Italy
Tel: (6) 59 40 29
Cable: HEWPACKIT Rome
Telex: 61514

FOR CANADIAN AREAS CONTACT:
Hewlett-Packard (Canada) Ltd.
275 Hymus Boulevard
Pointe Claire
Tel: (514) 697-4232
TWX: 610-422-3022
Telex: 01-20607

FOR AREAS NOT LISTED, CONTACT:
Hewlett-Packard
INTERCONTINENTAL
3200 Hillview Ave.
Palo Alto, California 94304
Tel: (415) 493-1501
TWX: 910-373-1267
Cable: HEWPACK Palo Alto
Telex: 034-8300, 034-8493

HEWLETT PACKARD

COMPONENTS